

SDR-3000 MRDP

Military Communications (MILCOM) Rapid-Prototyping Development Platform

cPCI



A fully integrated COTS “RF to Ethernet” black-side solution comprising RF and modem hardware, together with all software and tools for rapid SCA compliant radio development.

Benefits

- Uses field-proven technology selected by JTeL as the only COTS JTRS representative hardware set for JTRS waveform compliance testing
- Saves over 9 person-months of integration effort
- Supports multichannel radio development using a highly scalable and modular architecture
- Enables emulation of co-site interference
- Allows technology demonstrations in many airborne, maritime, and fixed environments
- Highly customizable

Applications

Tactical Military Communications

- Rapid Prototyping
- Waveform Development
- Verification and Validation testing
- Beamforming and MIMO research

Features

- Support for up to 4 independent channels, each operating in full or half-duplex mode between 0.5 MHz and 3 GHz, with IF bandwidths of up to 16 MHz
- Based on Spectrum’s SDR-3000 platform incorporating Xilinx® Virtex-II™ FPGA, Motorola MPC7410 PowerPC™ and TI TMS320C6416 DSP processing devices, all interconnected through high performance communications fabrics
- Support for both fast and slow hopping waveforms at up to 5000 hops/sec
- Includes a comprehensive sample application illustrating operation in a frequency agile environment
- GPS absolute time reference (IRIG-B and 10 MHz) with location
- Comprehensive training and support

Description

The SDR-3000 MRDP¹ is a fully integrated, black-side software defined radio (SDR) platform providing a commercial off-the-shelf (COTS) “RF to Ethernet” radio platform for military communications programs. It integrates a high performance fast tuning transceiver with a Software Communications Architecture (SCA)-enabled signal processing platform that has been adopted by the Joint Tactical Radio System (JTRS) Technology Laboratory (JTeL) as the only COTS JTRS representative hardware set. This integrated solution was designed specifically to derisk customers’ programs by providing the fastest route to developing SCA-enabled architectures and systems, waveform applications, and verification and validation platforms. The SDR-3000 MRDP is at technology readiness level six for many fixed, airborne, and maritime environments, making it suitable for field demonstrations and limited deployments.



Figure 1. SDR-3000 MRDP components: SDR-3001 and DRT2110

¹ Subject to U.S. and Canadian export regulations. Subject to U.S. International Traffic in Arms Regulations (ITAR).

Block Diagram

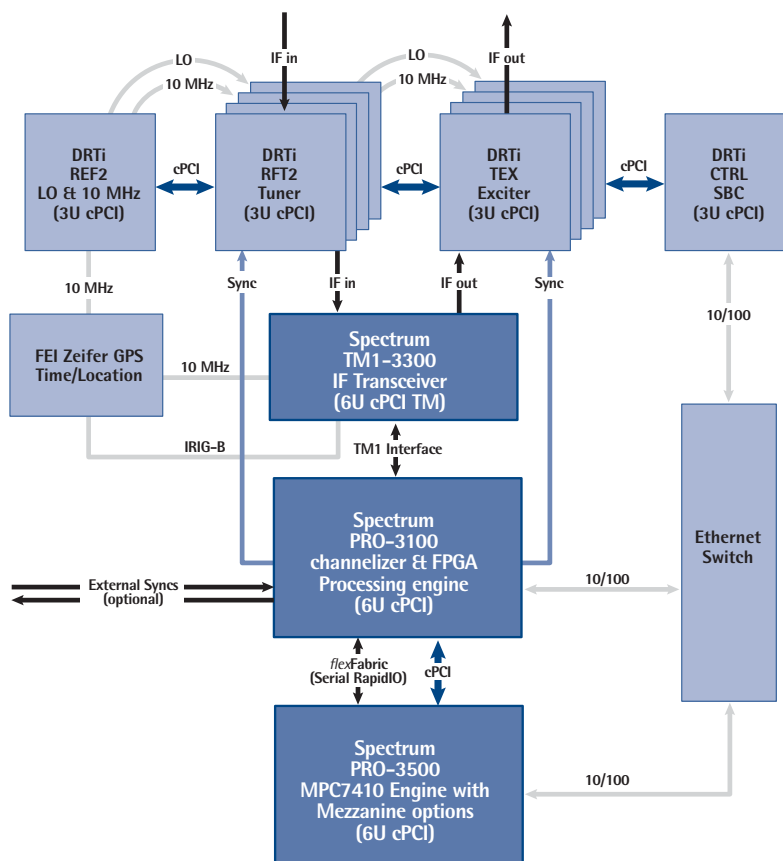


Figure 2. SDR-3000 MRDP System Architecture

Architecture

The SDR-3000 MRDP integrates a frequency agile RF transceiver subsystem, a high performance signal processing platform, and an SCA-enabled software operating environment into a scalable architecture for software defined radio applications.

[RF Transceiver Subsystem]

The RF transceiver subsystem consists of four basic elements from Digital Receiver Technologies, Inc., or DRTi, (www.drtd.com): an RFT2 tuner, a TEX exciter, a REF2 highly stable oscillator, and a DRTi CTRL single board computer. A variety of packaging options are available including the DRT2110 Wideband Tuner System. This subsystem integrates the elements above into a single 21-slot 3U CompactPCI chassis.

For more information or to order the DRT2110, please visit <http://www.drtd.com>.

[Signal Processing Platform]

The SDR-3000 signal processing platform was designed specifically for the requirements of software defined radio communications applications. It integrates heterogeneous processing elements (FPGAs, DSPs, and GPPs) seamlessly using a high performance embedded fabric. More details on the SDR-3000 can be found at www.spectrumsignal.com/products/sdr.

[Software]

In addition to the base software layers (Spectrum's *quicComm* and SCA BSP) offered in the RF subsystem and the SDR-3000 platform, the SDR-3000 MRDP provides other valuable software functionality:

- The Harris dmTK, an SCA core framework and development toolset, fully integrated onto the SDR-3000 MRDP platform
- Digital down converter (DDC) and digital up converter (DUC) FPGA cores interfacing to the IF
- An RF control API to manage all functionality of the RF subsystem
- A comprehensive dataflow example from the RF input, through the entire signal processing chain, and back out the RF output

In addition, Spectrum's Application Engineering Services team in Columbia, Maryland, USA can customize the SDR-3000 MRDP to modify existing or add additional features as required, such as:

- QPSK Mod & Demod
- TDM processing
- Polyphase resampling
- Channelization
- FSK Mod & Demod
- Frequency Hopping
- FFT

Operation

The RF subsystem is controlled using two methods: front panel Ethernet and SMA synchronization signals. A sockets-based control library running on a PPC communicates over the Ethernet interface to the CTRL SBC in the RF subsystem box. Frequency and attenuation commands are written and status is queried over this interface. In addition frequency tables may be loaded onto the TEX and RFT2. The Tuner and Exciter Sync signals allow for low latency and deterministic stepping through these frequency tables. Fine tuning of the frequency setting is achieved through a combination of coarse tuning of the RF subsystem and fine tuning of DDC and DUC cores on the FPGA processor. IF data flows through the FPGA processor allowing for precise control of data burst insertion or acquisition.

The system is designed to update the frequency table continuously in real-time. GPS absolute time via IRIG-B and 10 MHz reference are available and can be used to time stamp the incoming packets or to schedule outgoing packets. In addition, the system can be synchronized with external devices using optional External Syncs.

Customization

The supplied example application, including source code, shows the capability of the Radio System. Spectrum's Application Engineering Services (AES) team will help you map your application requirements to the platform and tailor the platform to your specific needs. In addition, the team's SCA expertise and application software/firmware components can be employed to speed your time to deployment.

Specifications

[export regulations]		The SDR-3000 MRDP is subject to the export control laws of the United States, including the United States International Traffic in Arms Regulations (ITAR).
[general]	RF Subsystem Processing Subsystem GPS	DRT2110 Spectrum SDR-3001 FEI Zeifer GPStarPlus
[analog I/O]	Rx IF Sample Rate Tx IF Sample Rate	80 MSPS at 14 bits 160 MSPS at 14 bits
[RF subsystem]	Rx RF frequency Tx RF frequency Rx IF bandwidth Tx IF bandwidth Tx frequency table size Rx frequency table size	0.5 MHz to 3 GHz 40 MHz to 2.9 GHz 30 MHz 16 MHz 500,000 entries 500,000 entries
[processing subsystem]	FPGA GPP DSP	Four Xilinx® XC2V6000 Two MPC7410 (more are optional), two IBM405 (more are optional) Optional Texas Instruments TMS320C6416 (two or four)
[external interfaces]	Rx Tuning Sync Tx Tuning Sync External Sync Ethernet RF Channels Absolute Time	5000 hops/sec (limited by RF receiver) 5000 hops/sec (limited by RF transmitter) LVTTL 10/100 BaseT Up to four channels, operating in full or half-duplex mode IRIG-B
[development software]	Operating System CORBA SCA Core Framework Example Applications	Wind River VxWorks v5.5 OCI TAO Harris dmTk v2.2.2.1 (SCA 2.2) RF Control library Modem Stack TDM/Hop Sequencer
[environmental]	RoHS	Please see component level datasheets for RoHS compliance or contact Spectrum Sales
[ordering information]	901-00041 901-00040	Contact your Spectrum Sales Representative for specific ordering information. SDR-3000 MRDP 1ST DEVELOPMENT SYSTEM SDR-3000 MRDP RECURRING PRODUCTION SYSTEM Note: To order the DRT2110, please contact DRTI directly at www.drty.com