

ePMC-FPGA*

Multi-Purpose I/O Processing Engine Enhanced PMC Module

ePMC



Benefits

- Flexible design platform
- High-speed, low latency, deterministic data paths to carrier board
- Supports multi-channel, multi-mode receivers for both narrowband and wideband air-interfaces, such as: CDMA, GSM, and W-CDMA
- FPGA application development accelerated by *quicWave*™ cores
- *quicComm*™ software architecture accelerates application development, simplifies the programming model, and ensures code portability

Applications

- Military communications and military satellite communications including wireless test and measurement, satellite earth station return link
- Signals intelligence including wireless surveillance, signal monitoring, array antenna applications such as direction finding and co-channel interference mitigation

Features

- Single-width Solano-based Enhanced PMC (ePMC) form factor
- Three Xilinx® Virtex FPGA devices, each providing up to 985,882 system gates
- Compatible with *quicWave* for Virtex-E cores
- High-speed mezzanine interface based on the Solano™ Communications IC
- 32-bit, 33 MHz PCI Host Bus interface
- Modular front panel I/O interface module, supporting a variety of I/O formats
- JTAG connector for compatibility with Xilinx ChipScope™ debugger

Description

The ePMC-FPGA is intended for use as a user-defined fast I/O device, a front-end signal processing engine, or a fixed-point or floating-point co-processor. The ePMC-FPGA is a single-width ePMC module, 32-bit, 33 MHz PCI device able to operate in a master or slave mode, with PCI burst DMA capability. The ePMC-FPGA is equipped with a modular front panel to support a variety of input formats. It offers three Xilinx XCV600E FPGAs for processing, as well as multiple output paths. A high-speed interface to the carrier board can be established via the Solano Communication IC. A PCI interface to the carrier board is also available.

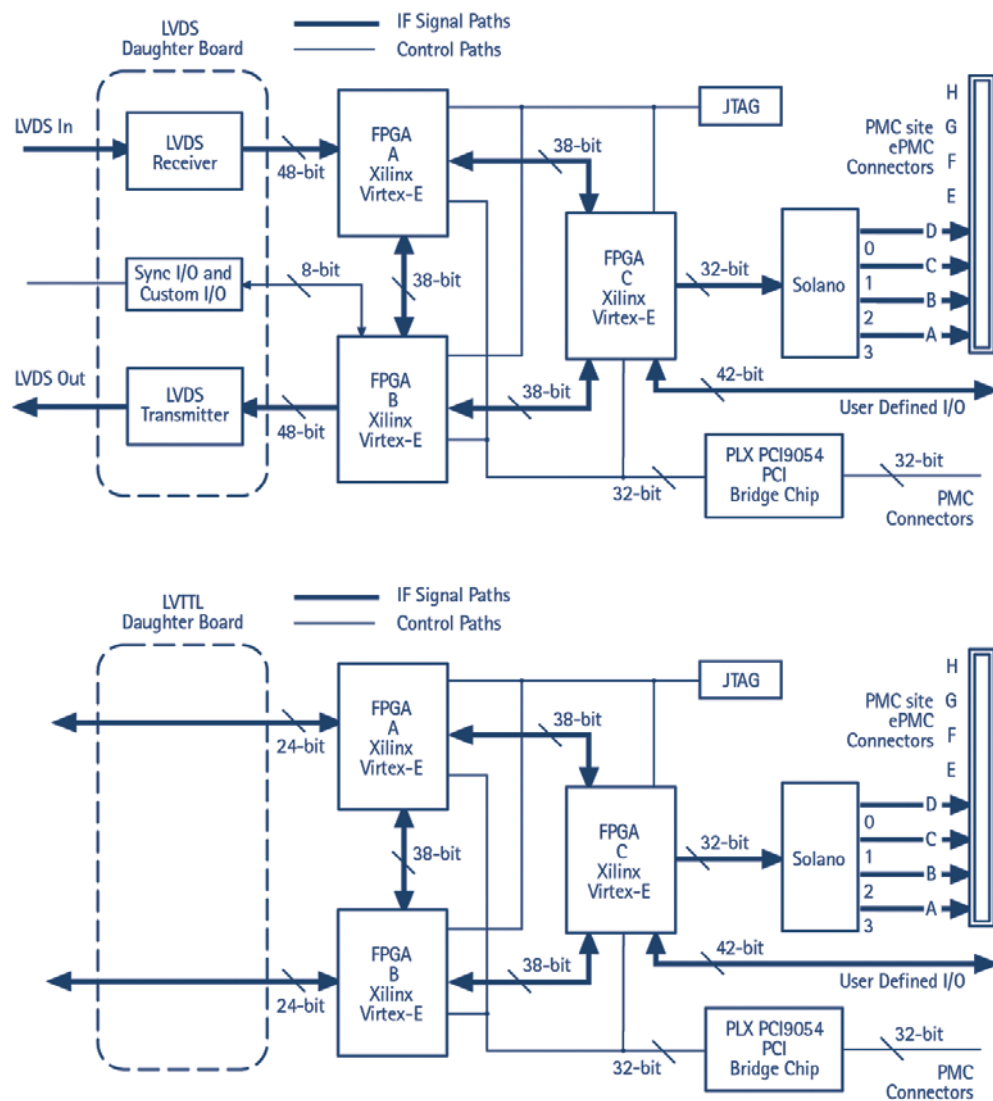
The ePMC standard adds the power of the Solano Communications IC to the PCI bus of the PMC standard. The addition of these high-speed communications channels enable 800 MB/s full-duplex of data throughput directly from the mezzanine to the processing engine. The ePMC-FPGA is fully compliant with the PMC standard IEEE 1386.1.

The ePMC-FPGA is compatible with Spectrum's ePMC-2ADC dual input 14-bit 65/80 MSPS A/D module and ePMC-8120 module, the Mosport Octal 'C6203 processing engine, the PRO-1900/1901 ePMC carrier boards and standard PMC modules, equipping users with a platform that is suitable for a wide variety of applications.



* For new designs, we recommend one of this module's successor products: XMC-8131, XMC-1131, or XMC-2131. For more information, please visit www.spectrumsignal.com/products/hcdr or contact Spectrum Sales.

Block Diagram



Architecture

The ePMC-FPGA has three Xilinx Virtex 600E FPGA chips (XCV300E and XCV400 devices can be delivered upon request). The ePMC-FPGA utilizes Spectrum's Solano Communications IC to provide up to 800 MB/s (full-duplex) of low latency, deterministic communications paths to Spectrum's signal processing engines.

The ePMC-FPGA PCI interface is implemented with a PLX9054 32-bit, 33 MHz I/O accelerator. This PCI bridge technology is able to operate in a master or slave mode, and supports PCI burst DMA transfers. The PCI bridge communicates directly with each FPGA in the system to allow configuration, command, and control of these devices over the PCI bus. Additionally, all the FPGAs have dedicated high-speed point-to-point communications paths to the other FPGA devices, allowing easy pipeline processing and algorithm partitioning.

[Solano Communications IC]

The Solano Communications IC provides high bandwidth data paths between ePMC mezzanine modules and ePMC carriers. It has four high-speed LVDS links each capable of 200 MB/s full-duplex. The four links give an aggregate bandwidth of over 1.6 GB/s per node. A data network implemented using this IC provides system throughput that can be many times higher than that offered by conventional based or serial link architectures.

[Xilinx Virtex-E FPGA]

The Virtex-E FPGA features a flexible architecture comprised of an array of configurable logic blocks and input/output blocks, all interconnected by fast routing resources. The Virtex FPGA is SRAM-based, and is customized by loading configuration data into internal memory cells. The XCV600E has 985,882 gates.

[Interfaces]

ePMC-FPGA incorporates a modular I/O interface supporting front-panel access in a variety of formats. Spectrum initially offers two I/O front panel interface module options for this product: a high-speed Low Voltage Differential Signaling (LVDS) interface and a user defined LVTTTL interface. The high-speed LVDS front panel module has two dedicated LVDS connectors (transmitter and receiver) that convert the data stream into 48-bit wide parallel data. A synchronization connector is also provided to allow the multiple modules to maintain synchronous operation for coherent applications such as beam forming and direction finding. The LVDS front panel interface is pin compatible with the ePMC-2ADC and ePMC-8120 modules.

The ePMC-FPGA LVTTTL front panel option communicates directly with two of the FPGA devices without any intervening active circuitry. This option provides 48 I/O pins, and gives the user the flexibility of configuring the pins as input, output or mixed input and output based on the requirements of the specific application.

Software

[FPGA Application Cores - *quicWave* for Virtex-E Cores]

quicWave for Virtex-E is a library of building blocks for the development of wireless modems and waveforms. These building blocks can be used standalone or combined with user-defined blocks to create a complete FPGA-based front-end processing implementation. An FPGA “wrapper” is supplied that abstracts all board level glue logic, such as the LVDS and PCI interfaces on the module. The “wrapper” is designed so users can expedite the integration of their custom cores into the ePMC-FPGA module.

[*quicComm* Software Development Kit (SDK)]

quicComm software equips users with basic link level access and control of Spectrum’s *flexComm*™ products. *quicComm* is standard across all *flexComm* products, allowing code portability. This software provides a board support package for control and data handling which:

- Allows configuration and control of the Solano~links and the ePMC modules
- Initiates and manages data transfers
- Manages interrupts
- Enables dynamic loading on a processor without affecting other processors

Specifications

[general]	FPGA Device	Three Xilinx Virtex 600E devices per board. XCV300E/XCV400E can also be supported.
[buses]	Host	32-bit 33 MHz PCI Bus Interface
[external interfaces]	PCI Interface	PLX9054 32-bit, 33 MHz PCI I/O accelerator
	LVDS I/O	48-bit LVDS high-speed user-changeable Front Panel interface, compatible with Spectrum's ePMC-2ADC and ePMC-8120 modules
	LVTTTL I/O	48 user-programmable I/O and 4 dedicated clock input signals routed to the user changeable Front Panel interface
	JTAG Connection	JTAG connector for Virtex FPGA for compatibility with Xilinx ChipScope™ debugger
	ePMC Interface	Four Spectrum Solano~links, each providing over 200 MB/s (full-duplex)
	User Defined I/O	A user defined interface is provided from FPGA C to the JN4 connector
[compatibility]	Carrier Compatibility	Mosport 'C6203 processing engine and the PRO-1900/PRO-1901 carriers
	Operating System	Refer to carrier specifications
[development software]	Application Libraries	<p>quicComm Software Development Kit provide functions for:</p> <ul style="list-style-type: none"> • Configuration and control of ePMC-FPGA • Initiating PCI or LVDS data transfers • Programming Solano Communications IC for high-speed data transfers • Programming of the on-module FPGAs
	Example Code	<p>Example code provides a starting point for rapid software prototyping</p> <p>Examples include:</p> <ul style="list-style-type: none"> • ePMC-FPGA initialization • Verilog code example to demonstrate a straight-through data path • Data read through the PCI bus and Solano~links
[other software]	FPGA Code Development	Alliance tools from Xilinx and Synplify Synthesis® from Synplicity are required for the FPGA code development
	FPGA Cores	A variety of FPGA cores are available, including both wideband and narrowband digital receiver cores. Contact Spectrum sales for details.
[electrical]	Power	Supply Voltage +5V, 3.3V +/-5% (supplied by PMC connector) A 1.8V on-board supply for the FPGA core power is derived from the 5V supply
	Current Consumption	Typical: 1.32A at +3.3V and 3.5A at + 1.8V
[mechanical]	Size	149 mm (height) x 74 mm (width)
	Modules	Single-width form factor in compliance with IEEE P1386.1 PMC Standard
[environmental]	Temperature	Operating temperature range of 0 to 50° C Storage temperature of -20 to 85° C
	Humidity	10 to 80% non-condensing
	RoHS	0 of 6 compliant. For other RoHS options, please contact Spectrum Sales.
[ordering information]		For new designs, we recommend one of this module's successor products: XMC-8131, XMC-1131, or XMC-2131. For more information, please visit www.spectrumsignal.com/products/hcdr or contact Spectrum Sales.
	650-00075	ePMC-FPGA-XCV600-LVDS MODULE with Interconnect Modules
	100-00347	ePMC-FPGA-XCV600-LVDS Wideband Digital Down Converter Image and documentation
	100-00346	ePMC-FPGA-XCV600-LVDS Narrowband Digital Down Converter Image and documentation
	100-00493	HCDR-10XX SDK
	202-00198	ePMC-FPGA-LVDS Cable Kit
[custom configurations]		For custom configuration options, please contact Spectrum sales for details