SPECTRUM SIGNAL PROCESSING BY VECIMA

PRO-4610

Dual Analog IF Transceiver Processing Module

3U cPCI

flexComm

Benefits

- Rugged design to support deployment in harsh environments at extended temperature ranges
- Cost-Effective I/O and Processing to support Multi-Channel, Gateway, MIMO, and Smart-Antenna applications
- Optimized for wireless modem applications requiring low latency and high data throughput
- Maximize system extensibility with modular architecture and data flow routing strategies
- Accelerate application development, simplify the programming model and ensure code portability with *quic*Comm™ API, common across all *flex*Comm™ products
- Rapid optimization of size, weight, power and cost to meet fielded application or program requirements. Spectrum's Modified COTS process reduces your time to deployment by up to 2 years

Applications

- Tactical Military Communications (MILCOM) - ground vehicular, airborne, unmanned aerial vehicles (UAV) and shipborne
- Electronic Warfare (EW) including Electronic Attack - jamming
- Military Satellite Communications (MILSATCOM) Terminals
- Other high-end signal processing applications including MIMO, or Beamforming

Features

- 3U CompactPCI® form factor
- Available in conduction-cooled and air-cooled versions.
- Dual IF-to-Digital Conversion at 14-bits resolution, up to 105 MSPS
- Dual Digital-to-IF Conversion at 14-bits resolution, up to 300 MSPS
- Ultra-low additive jitter of less than 800 femtoseconds
- Two 12-bit, 100 KSPS D/A converters for external AGC
- Four 12-bit, 100 KSPS A/D converters for RSSI sensing
- High-speed serial backplane I/O for inter-board communication
- Xilinx® Virtex-4™ technology for wideband processing and low power operation
- TMS320C6416T DSP for baseband processing and compatibility with legacy waveforms
- Extensive backplane General Purpose I/O for interface and control
- FPGA "wrapper" abstracts board-level logic to accelerate FPGA application development
- Green Hills® INTEGRITY® Real-Time Operating System with MULTI® and Wind River® VxWorks® with Tornado® (optional)
- Spectrum's *quic*Comm™ API hardware abstraction layer
- Software Communication Architecture (SCA) Core Framework Support

Description

The PRO-4610 is a key component in Spectrum's SDR-4002 Multi-Channel Radio Subsystem (MRSS). It combines two analog-digital-converters, two digital-to-analog converters, a Virtex-4 FPGA, and a TMS320C6416T DSP to support the physical layer processing requirements of many legacy and wideband networking waveforms. The PRO-4610 features high-speed serial backplane links that provide high-bandwidth communications with the PRO-4600 Modem Processing Engine and other PRO-4610 Dual Analog IF Transceivers.

Figure 1. PRO-4610 available in conduction-cooled and air-cooled versions

Block Diagram

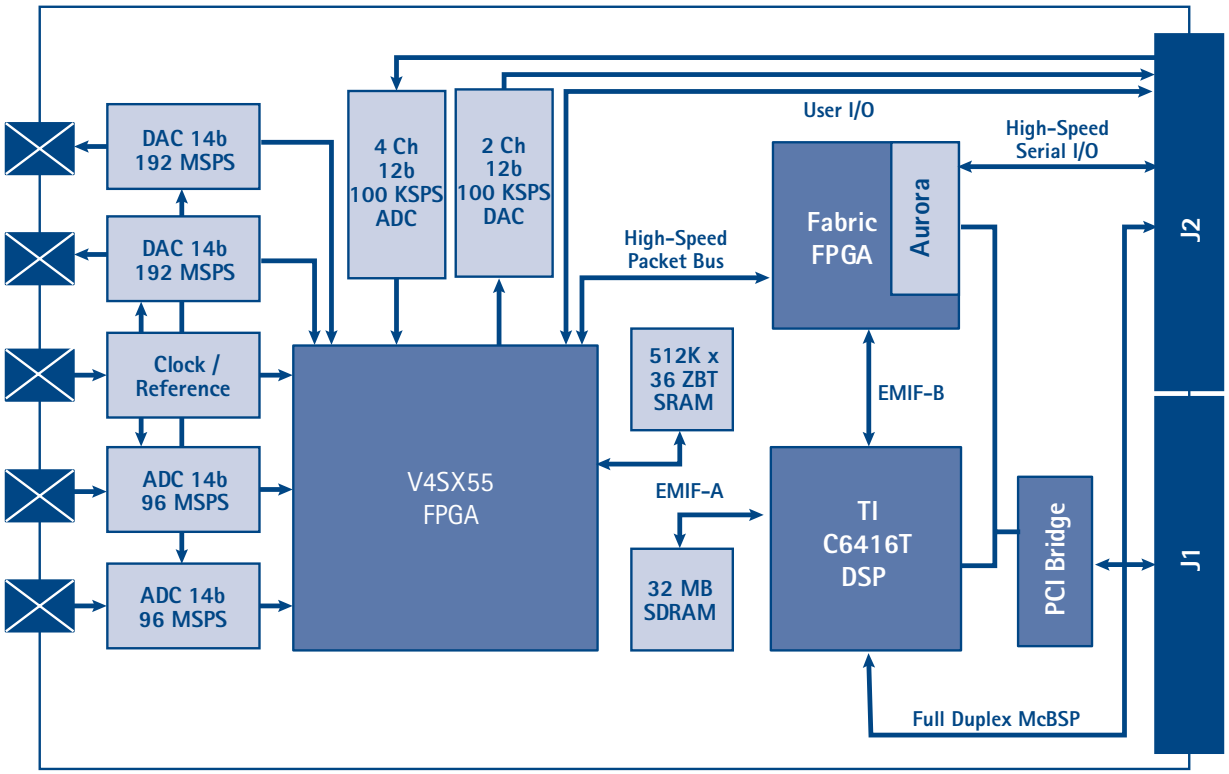

Figure 2. PRO-4610 Block Diagram.

Architecture

The PRO-4610 is a commercial-off-the-shelf (COTS) 3U software radio modem processing engine that is ideal for Tactical MILCOM and other communications applications. Its scalable, modular hardware/software architecture allows for quick modification and adaptation to unique program requirements, thus substantially reducing the high expense and risk associated with developing your own hardware.

The PRO-4610 is a key element of the SDR-4002 Multi-Channel Radio Subsystem (MRSS), and provides analog IF conversion, and physical and MAC layer processing functions. It is intended to be used in conjunction with a PRO-4600 Modem Processing Engine and a SSP-4910 cPCI controller. Refer to SDR-4002MRSS datasheet for intended configurations.

The PRO-4610 combines dedicated high throughput, low latency data paths with heterogeneous processing capability and a highly focused software stack, which includes Spectrum's *quic*Comm API. Support for an SCA core framework and CORBA ORB are optional.

[A/D and D/A Converters]

The PRO-4610 uses two AD6645 14-bit ADCs, sampling at 96.0 MSPS and supports a range of sampling rates of 36 MSPS up to 105 MSPS. The input includes an AC (transformer) coupled circuit that has a passband of 0.5 MHz to 250 MHz. The PRO-4610 uses two AD9755 14-bit DACs sampling at 192.0 MSPS standard and supports sampling rates of up to 300 MSPS. 300 MSPS is supported as an option*, and requires special synthesis tools. Contact Spectrum Sales for details.

[Ultra Low Additive Jitter]

The PRO-4610 clock circuitry design incorporates techniques to minimize "additive" jitter (phase noise) that is essential to maximize the energy per bit/noise spectral density ratio (Eb/No), improving the overall performance of a digital communications system. Radios designed to maximize Eb/No provide significant benefits to the end-user, including increased communications range and improved payload data throughput. The PRO-4610 "additive" jitter is less than 800 femtoseconds (800×10^{-15} seconds) "additive" to the jitter spec of other system components such as an external reference clock. For internally sampled PRO-4610s with no external references, the total jitter is less than 800 femtoseconds.

* See future options section of this datasheet.

[Analog Channel Balance]

The PRO-4610 is engineered to minimize phase and amplitude imbalance between ADC channels. This is a prime characteristic of the PRO-4610 design that is essential to maximize SFDR and image rejection performance for MIMO radios. Phase imbalance, commonly known as “skew”, is minimized in the ADC pairs and the DAC pairs.

[High-Speed ADC/DAC Clock Options]

The PRO-4610 high-speed ADC/DAC sampling clock supports input from an industry standard 10 MHz internal or external reference clock. In addition to this, the PRO-4610 allows input of an external sampling clock which may range from 36 MHz to 210 MHz. The standard product PRO-4610 clocks the DAC at 192.0 MHz, twice the ADC rate of 96.0 MHz. Alternate sampling rates are supported as an optional feature.*

[Additional Interfaces]

Four 100 KSPS ADCs and two 100 KSPS DACs are available to provide control of an RF front-end. For example, an analog signal generated from the RF front-end may be digitized in the ADC for the purpose of received signal strength indication (RSSI) or a DAC may be used to output an AGC signal. These converters can alternatively be used to support other off-board peripherals. In standard configuration, two ADCs have a low-pass filter at 3 kHz. As a future option, the low-pass filter may be extended up to 30 kHz or removed entirely. The DAC output is unfiltered.

[User Programmable FPGA]

The Xilinx Virtex-4 FPGA platform is ideally suited for high-performance IF and baseband signal processing tasks inherent in tactical MILCOM applications such as channelization, network synchronization, carrier and baud recovery and resampling. On the PRO-4610, a Xilinx Virtex-4 SX55 is available for user programming. Power consumption of the Xilinx Virtex-4 is reduced by up to 50% over comparable Virtex-II Pro™ FPGAs using Xilinx’s Triple-Oxide Technology. The PRO-4610 ships standard with an SX55 FPGA. Virtex-4 LX100 and LX160 FPGAs are future options*.

Device	4SX55	Estimated Resources Available to the Application
Logic Cells	55,296	44,230
Block RAM (Kbits)	5,760	5,526
DSP Slices	512	512
Digital Clock Management Blocks	8	3

Figure 3. User programmable FPGA attributes and estimated resources available to user.

[TMS320C6416T DSP Processor]

A 600 MHz TMS320C6416T processor provides low power consumption baseband processing, as well as providing support for legacy waveform code. The C6416T DSP is connected with 64 MB of SDRAM. The DSP is connected to the fabric FPGA crossbar allowing flexible, high-performance channelized data flow.

[Overall Data Flow]

In order to facilitate highly flexible, yet high-performance communications, the PRO-4610 architecture uses a fabric crossbar. This provides dedicated, high throughput, low latency data paths between all processors and the most important external data interfaces. A separate “soft real-time” data path is provided via the on-board PCI bus that is primarily used for control. By isolating signal from control, determinism and performance is assured. In addition, a hardware interrupt scheme is provided, allowing tight synchronization between the user programmable FPGA and the DSP.

[Serial I/O Backplane Links]

The PRO-4610 supports four serial I/O links to the rear panel that are typically used to interface to a PRO-4600 modem processing engine, another PRO-4610, or to an RF front-end. These links support the Xilinx Aurora protocol, however other protocols such as serial FPDP, serial RapidIO or other custom protocols may be implemented as an option.* The serial links can be used to create larger systems of collaborating PRO-4600 and PRO-4610 boards such as in the SDR-4002MRSS. Each serial link is capable of supporting data rates at up to 220 MB/s full-duplex. In an air-cooled chassis, the high-speed serial links can be routed from the cPCI J2 connector to rear-panel SLINK connectors via the TM2-4900 Rear Transition Module, and can be routed between boards using SLINK cables. In a conduction-cooled chassis, these signals would normally be routed via the backplane, such as the BP1-3911, or BP1-3910 used in the SDR-4002MRSS configuration.

* See future options section of this datasheet.

[General-Purpose I/O (GPIO)]

A number of GPIO lines are provided to facilitate user-defined communications to external devices. These include:

- Five differential pairs (LVDS or LVCMOS 2.5V) to the user FPGA
- Twenty-five user FPGA single-ended (LVCMOS 2.5V or LVTTL) to the user FPGA*
- One multi-channel buffered serial port (McBSP) line to the DSP

The differential pairs are capable of running at a rate up to 213.3 MHz while the single ended lines are suitable for lower speed information. Typical uses of GPIO include controlling the RF front-end using automatic gain control (AGC), frequency hop synchronization between the modem and RF stages, time code input from a GPS receiver, and sync distribution between slots, or push-to-talk (PTT) control signal distribution.

[cPCI Bus]

In order to facilitate control and communication with other system boards, a 32-bit/33 MHz PCI bus interface to the cPCI backplane is provided.

[Operation in Rugged Environment]

In order to address tactical military needs for harsh environments, the PRO-4610 is designed in accordance with ANSI/VITA 47 CC3 to support conduction cooling, extended temperature range, and increased shock and vibration immunity using embedded stiffening, heat sinks and wedge locks. For protection against high levels of humidity and other environmental contaminants, the PRO-4610 can be conformally coated with a protective sealant. Temperature sensors are mounted to allow the software application to monitor the temperature of the "hot" components.

[Modified COTS Optimization]

The PRO-4610 hardware and software architecture is based on Spectrum's Tactical MILCOM reference designs resulting in a quick turn-around to optimize the product to meet the size, weight, power, cost and/or ruggedization characteristics of fielded applications. In addition to this, the PRO-4610 supports independent hard and soft real-time communications fabrics that allow the use of custom data-routing techniques. Using the Modified COTS (MCOTS) process, Spectrum works with its customers to provide an MCOTS solution while substantially minimizing the time-to-deployment. For more information on the benefits of Spectrum's MCOTS process, please contact Spectrum Sales.

Software

[*quic*Comm]

The PRO-4610 software interface is via a *quic*Comm Software Development Kit (SDK) that is available on all supported platforms. *quic*Comm software abstracts the underlying hardware providing users with basic transport level access and control of Spectrum's *flex*Comm products. This significantly accelerates user application development.

*quic*Comm is standard across all *flex*Comm products, allowing code portability. This software includes a board support package for control and data handling which allows:

- Configuration and control of the data links between processors and mezzanine cards
- Initiation and management of data transfers
- Interrupt management, and
- Application loading onto the DSP and user programmable FPGA.

*quic*Comm is also implemented on the DSP which provides access to the external interfaces, and support for control and data handling from within your DSP application.

* See future options section of this datasheet.

Spectrum provides software examples with the PRO-4610 SDK, and system-level examples with the SDR-4002MRSS including:

- Analog loopback using the User FPGA and DSP
- System analog loopback using two PRO-4610 modules (one as input, one as output) and one PRO-4600 module intermediary

The above examples provide application developers with a basis to commence their own application software. This benefits the developer to obtain quick familiarity with data flow details resulting in substantial time-savings upon the commencement of application development. For more information on *quic*Comm, please consult the *quic*Comm datasheet.

[FPGA Wrappers]

As a part of Spectrum's *quic*Comm package, an FPGA wrapper is provided to abstract all board level interfaces on the Virtex-4 FPGA, including the interfaces to the analog converters, communication fabrics and control. The wrapper is designed so users can expedite the application integration onto the PRO-4610. See Figure 3 "User Programmable FPGA Attributes" which shows an estimate of the FPGA resources available for the user.

[FPGA Tool Flow]

Although other tools can be used, the PRO-4610 is designed to support a combined Synplify Pro/Xilinx ISE Foundation™ tool flow. ISE is an integrated programmable logic design environment that includes schematic capture, power analysis tools, physical synthesis for FPGAs, advanced Place and Route Algorithms, and COREgenerator, a graphical interactive design entry tool that is used to create high-level modules. Synplify Pro is a high-performance, sophisticated logic synthesis engine that utilizes proprietary Behavior Extracting Synthesis Technology® (B.E.S.T.™) to deliver fast, highly efficient FPGA and CPLD designs. The Synplify product takes Verilog and VHDL Hardware Description Languages as input and outputs an optimized netlist in most popular FPGA vendor formats. Xilinx's System Generator tool can also be used to graphically design, simulate, and generate FPGA-based algorithms within the Simulink environment from The MathWorks.

[Operating System]

The PRO-4610 is designed to operate with at least one PRO-4600 Modem Processing Engine to provide system control functions. The PRO-4610 supports the Green Hills INTEGRITY real-time operating system (RTOS, which is designed for use in embedded systems that require maximum reliability.

Using Spectrum's MCOTS process, SDR-4000 is capable of fast optimization to support other real-time operating systems such as Wind River VxWorks, or Linux.*

[Software Communications Architecture (SCA)]

The SCA is an open specification sponsored by the U.S. Department of Defense Joint Tactical Radio System (JTRS) program. It specifies software, hardware, security and networking architecture requirements for open, programmable software defined radio (SDR) systems with flexible, re-programmable communication capabilities. The SCA specifies a common framework to build-up, configure, connect and tear down distributed, embedded radio applications while maximizing waveform portability. An SCA core framework is available for order as an option. Please contact Spectrum Sales for more information.

Services

[Customer Training]

Spectrum's training workshops are designed to get your team up and running in the shortest time possible by using a combination of lectures and at least 60% hands-on experience with your system. Experience thus far has shown this service to be an invaluable tool that generates significant cost savings and reduces risk for Spectrum customers.

The standard SDR-4000 training consists of two days with a Spectrum Applications Engineer working with actual hardware. An additional two day course that covers the SCA Core Framework and SCA BSP is available. Application integration consultation is also available. Training can be done either at Spectrum's headquarters in Burnaby, B.C., Canada or at the customer site. For complete details, please see the training datasheet.

* See future options section of this datasheet.

[General]

- FPGA Device Xilinx Virtex-4: XC4VSX55
- External Reference Oscillator: 0.75 - 1.6 Vpp 10 MHz sample clock reference
- Internal Reference Oscillator: 10 MHz sample clock reference
- External Sampling Clock: Supports range of 36 MHz to 210 MHz, 0.75 - 1.6 Vpp
- DSP processor: 600 MHz TMS320C6416T processor with 64 MB of SDRAM

[Analog I/O]

- A/D Converter: Two Analog Devices AD6645 14-bit @ 96.0 MSPS (alternate sampling rates 36 to 105 MSPS are optional)
- ADC Input: AC coupled, full scale 1.29 Vpp into a 50 ohm load @ 70 MHz IF, 3 dB input bandwidth: 500 kHz – 250 MHz
- D/A Converter: Two Analog Devices AD9755 14-bit @ 192.0 MSPS (alternate sampling rates up to 300 MSPS are optional)
- DAC Output: AC coupled, max 0.47 Vpp typical into a 50 ohm load @ 70 MHz, 3 dB output bandwidth: 500 kHz – 80 MHz
- ADC SFDR @ 96.0 MSPS, -1 dBFS input;
  - 10.7 MHz IF (10 MHz b/w) > 90 dB SFDR typical;
  - 21.4 MHz IF (10 MHz b/w) > 85 dB SFDR typical;
  - 70.0 MHz IF (30 MHz b/w) > 80 dB SFDR typical
- DAC SFDR @ 192.0 MSPS, single tone -1 dBFS;
  - 10.7 MHz IF (10 MHz b/w) > 90 dB SFDR typical;
  - 21.4 MHz IF (10 MHz b/w) > 90 dB SFDR typical;
  - 70.0 MHz IF (30 MHz b/w) > 82 dB SFDR typical
- SFDR note: SFDR measurements may vary from the above based on IF frequency, sampling rates, method of tone generation and other signaling criteria
- Jitter less than 800 femtoseconds additive jitter through the analog clock distribution circuitry
- Low speed: A/D Converter Quad 100 Ksps (ENOB of 10.5b filtered, 9.6b unfiltered)
- Low speed: D/A Converter Dual 12-bit @ 100 Ksps (unfiltered)

[External Interfaces (via Rear Transition Module)]

- Analog Input/Output SMA receptacle 50 ohms
- External Reference Oscillator SMA receptacle 50 ohms
- Host cPCI Bus: 32 bit/33 MHz cPCI interface
- JTAG Connection: JTAG connector for Virtex-4 FPGA, Xilinx Chipscope™ debugger compatible
- GPIO: 4 differential LVDS pairs and 25 single-ended LVCMOS lines are available via the J2 connector. LVTTL as an option
- High-speed serial: Four Aurora links to the cPCI J2 connector (220 MB/s sustained per link full duplex)

[Compatibility]

- Supported: Spectrum PRO-4600 Modem Processing Engine
- Operating System: Green Hills® INTEGRITY® or Wind River® VxWorks® (optional)

[Development Software]

- Application Libraries *quic*Comm Software Development Kit
- FPGA Code Development ISE Foundation tools from Xilinx, and Synplify Pro from Synplicity is required
- HDL Coding Language: VHDL
- TI Code Composer Studio and DSP BIOS

[Electrical]

- Supply Voltage (DC) Supply Voltage +5V, 3.3V, +12V, -12V, +5% / -3% (supplied by cPCI J2 connector)
- Power estimate 19 watts includes FPGA wrappers, receiving and transmitting (2 x DACs and 2 x ADCs). Power estimates do not include User application code

[Environmental]

- Operating Temperature Air-cooled: Operating temperature range of 0 to 50° C, forced air @ 600 LFM
- Industrial conduction-cooled: -40 to +70° C card edge compliant to ANSI/VITA 47
- Shock and Vibration: conduction-cooled version designed to meet MIL-STD-810F (ANSI/VITA-47 ECC3 levels)
- Conformal Coating Optional. Contact Spectrum Sales for details
- RoHS 5 of 6 compliant (Pb solder exemption).
  For RoHS ordering information, other RoHS compliance options or certificates of compliance, please contact Spectrum Sales

[Ordering Information]

- 650-00598: PRO-4610-SX55-AC Dual Analog IF Transceiver
- Designed for use in the SDR-4002 MRSS. Please contact Spectrum Sales for assistance in selecting the correct configuration

[Custom Configuration]

- For custom configuration, please contact Spectrum Sales

[Future Options]

Future options may be implemented at the discretion of Vecima Networks Inc. or its subsidiaries based on market demand.**

- Alternate User FPGA size Virtex-4 LX100/LX160
- Alternate Sampling Rates High-speed DAC up to 300 MSPS, ADC up to 105 MSPS
- Built-In-Test PBIT, IBIT and power-up, offline and background diagnostics including loop-back tests and libraries for writing custom BIT routines

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