



A COTS integrated “IF-to-Ethernet” platform for the development and deployment of wideband Electronic Support (collection) and Electronic Attack (jamming) systems with up to 6 IF inputs and outputs covering a total of up to 480 MHz of bandwidth

Benefits

- Save months of hardware development and integration effort
- Save months of effort in software infrastructure and application development
- Spend your engineering dollars on the algorithm and application rather than building processing and data flow architecture
- Save time and effort by developing directly on the ruggedized deployment target
- Easily scaled down for lab use

Applications

- Wideband and/or multichannel signal collection and processing
- Jamming of frequency agile signals across a bandwidth of up to 480 MHz

Features

- 6 intermediate frequency (IF) inputs and outputs, each supporting up to 80 MHz bandwidth
- Internally clocked, with interfaces for external 10 MHz Reference and external IRIG-B timestamping
- Low latency digital control bus interfaces for RF front-end and power amplifier
- Gigabit Ethernet output data pipe for real-time mass storage of received channels
- Includes overall data flow example with source code and other relevant test example code
- Supports semi-rugged operation appropriate for deployment in various tactical environments including vehicle-mounted deployments
- Optional extended humidity tolerance (via conformal coat of all boards)
- Comprehensive training and support

Description

The SDR-3002 EWRDP¹ is a fully integrated, commercial off-the-shelf (COTS) “IF-to-Ethernet” platform for the development, prototyping and deployment of Electronic Support and Electronic Attack applications. The platform has 6 channels of coherent IF input and output covering a spectrum of up to 480 MHz of bandwidth, with ample FPGA and General Purpose Processor (GPP) processing capability. The system has additional LVTTTL digital I/O for the control of RF front-ends and power amplifiers and a Gigabit Ethernet link capable of data output (e.g., to a separate analysis PC or to a storage device) at sustained rates in excess of 50 MB/s. A system software data flow example demonstrating the data rates is provided as part of the package. Suitable for deployment in many harsh environments and at temperatures up to 50°C, this flash-bootable, 11U-high system can meet the needs of stationary and mobile collection and jamming applications. The system boards can be conformally-coated for operation in high humidity environments. In addition, a smaller 2U-high, 2 channel version is available for lab development and for use in smaller scale systems in more benign environments.



SDR-3002 EWRDP

¹ Subject to Canadian export regulations. Not subject to U.S. International Traffic in Arms Regulations (ITAR).

Block Diagram

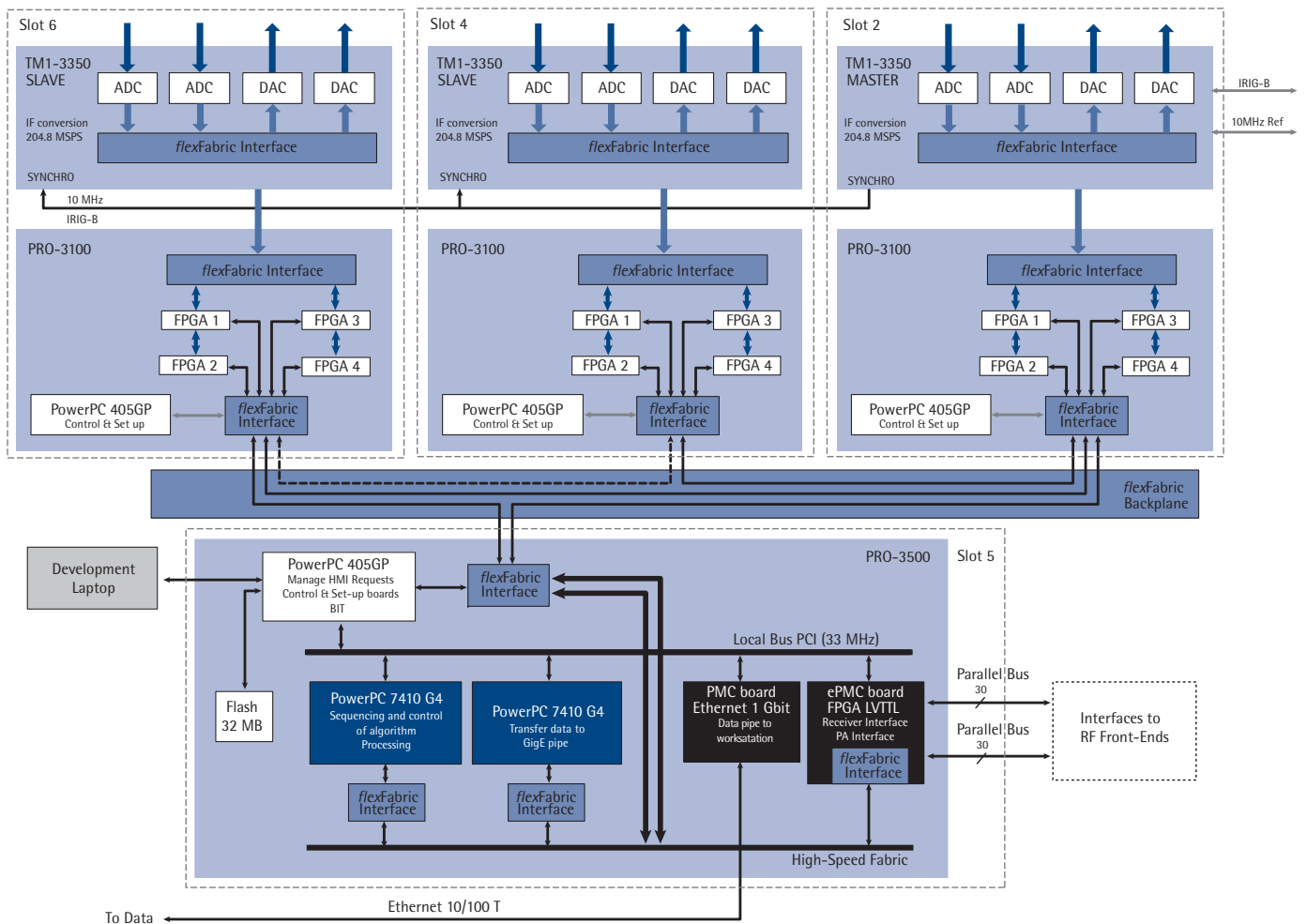


Figure 1. SDR-3002 EWRDP Block Diagram

Architecture

The SDR-3002 EWRDP is based on Spectrum's proven 6U cPCI SDR-3002 software defined radio platform that has been available for several years and designed into multiple programs and applications. The system is comprised of three identical slots, each containing:

- Two channels of analog IF input (on the transition module),
- Two channels of analog IF output (also on the transition module), and
- A quad FPGA processing engine (in the cPCI slot)

Finally, one additional slot containing a card with baseband processors and digital and Gigabit Ethernet interfaces rounds out the system configuration.

The cards communicate over PICMG 2.16-compliant backplane switched Ethernet for set-up and ongoing control activities, while hard real-time high-speed data transfer is facilitated over a high-speed *flexFabric* backplane. The system is housed in an 11U rugged chassis, with two 600W power supplies, a PICMG 2.16 backplane switch card and two large fans. All I/O is routed to a rear breakout panel. The chassis can fit into a 19" rack.

The IF interfaces are provided by 3 of Spectrum's TM1-3350 204.8 MS/PS 12-bit ADC/14-bit DAC modules. Each module has its own on-board 204.8 MHz clock oscillator. One of the modules, designated as a 'master' TM1-3350 module, has interfaces for an external 10 MHz reference and IRIG-B signal, and distributes these signals to the other two TM1-3350 modules, ensuring synchronization of the sampled and digitized data across all the cards and allowing coherent channel processing. Data flows from each TM1-3350 directly to FPGAs on an associated Spectrum PRO-3100 Virtex-II FPGA processing engine card over an internal fabric interface with a deterministic latency. Following processing in the FPGAs, the data can be sent over the high-speed fabric to other PRO-3100 FPGA boards or to the Freescale™ MPC7410 PowerPCs on the PRO-3500 baseband processing engine card. One of these 7410s is associated with controlling the LVTTTL digital bus (two sets of 30 signals) for communication with an RF front-end and power amplifier; the other 7410 with shipping data over the Gigabit Ethernet port. The digital bus is implemented via Spectrum's ePMC-FPGA mezzanine module sitting upon one of the PRO-3500 ePMC sites. The Gigabit Ethernet port is implemented using another mezzanine card on the second ePMC site.

The overall system can be accessed via a separate 10/100 Ethernet port connected into an external Ethernet on the PICMG 2.16 switch card. This network connects to the IBM 405GP processors on each of the PRO-3100 and PRO-3500 cards, and the 7410 processors. During development, a laptop (provided) is connected via this port to facilitate platform booting, code uploading, debugging and user interaction. The laptop can also be used as a human-machine interface during deployment, although the system can be configured to boot from flash instead of the laptop, if preferred.

Further details about the individual SDR-3002 components (PRO-3100 FPGA processing engine, PRO-3500 baseband processing engine, TM1-3350 wideband analog I/O module, and the ePMC-FPGA I/O processing module) can be found at Spectrum's website, www.spectrumsignal.com.

Additional Hardware

[Gigabit Ethernet PMC]

The Gigabit Ethernet interface is implemented using an XGE4010 PMC from Critical I/O sitting on the PRO-3500 card's mezzanine site. The XGE4010 is an intelligent module with a hardware protocol offload engine which takes care of implementing the Gigabit Ethernet protocol. A Spectrum *quicComm*[™] API library is used to access the card. For more information on the XGE4010 PMC, visit www.criticalio.com.

[PICMG 2.16 Backplane Ethernet Switch]

The backplane Ethernet switch is a GE Fanuc Embedded Systems' CP946 card. The CP946 is a 24 + 2-port Layer 2 switch with 24 10/100 BaseTx ports routed to back panel and 2 1000 BaseTx ports routed to front panel. The card requires no software set-up in the SDR-3002 EWRDP system, although advanced functionality is provided by the card, if required. For more information on the CP946 card, visit www.gefanuc.com.

Software

[Examples with source]

The system runs on Wind River® VxWorks® real-time operating system with Spectrum's *quicComm* Application Programming Interface (API) abstraction layer. Beyond the physical hardware and software integration, the provision of highly relevant application data flow examples, along with source code, provides a key time saving benefit. The examples provided include:

- 6-channel synchronization demonstrating the IRIG-B timestamping and how it is used to coherently sample 6 channels of ADC input.
- Overall system data flow demonstrating 5 ADC channels sampling at 204.8 MSPS, each sending data to a different FPGA where it is decimated to a rate of about 8 MB/s per stream, sent to one of the 7410 processors, and then forwarded out over Gigabit Ethernet. This flow is representative of a wideband application that breaks a bandwidth into smaller overlapped blocks and integrates all the data on one processor for combined processing of the entire bandwidth.
- Overall system data flow demonstrating the same data flow as above, but with the system booting from flash memory, rather than relying on pulling boot files from an attached PC over Ethernet.
- Single channel data flow out Gigabit Ethernet demonstrating a single channel version of the overall data flow with the output data flowing out of the Gigabit Ethernet port at a sustained rate of 50 MB/s.

[*quicComm* Software Development Kit (SDK)]

quicComm is a high-performance software development tool that provides an API for interprocessor and I/O-to-processor communications. *quicComm* is a standard on Spectrum's products and spans all of our processing technologies, including DSPs, GPPs, interfaces to FPGAs and I/O. *quicComm* enables developers to rapidly create multiprocessing communication applications with a mixture of processing engines, communication fabrics and I/O devices. *quicComm* provides:

- Configuration and control of the high-speed fabric links between the processors and between mezzanine sites
- Initiation and management of data transfers
- Management of interrupts
- Dynamic loading on a processor without affecting other processors
- FPGA wrappers to abstract all board level interfaces on each FPGA, including the interfaces to the analog converters, communication fabrics and control. The wrapper is designed so users can expedite the integration of third-party or custom FPGA IP cores.

Please see the *quicComm* datasheet for more details.

[Development Laptop]

A Microsoft® Windows® XP development laptop can be ordered as an option. This PC is delivered with all the necessary cabling interfaces to the SDR-3002 EWRDP, such as the JTAG emulator pods for the FPGAs and Ethernet connection. XP Server software is pre-loaded on this laptop for communication with the SDR-3002 EWRDP allowing development to begin immediately. Microsoft Visual Studio .NET is also included to provide an integrated development environment for Windows-based control code.

Specifications

[export regulations]		The SDR-3002 EWRDP is subject to the export control laws of Canada. The SDR-3002 EWRDP is NOT subject to the United States International Traffic in Arms Regulations (ITAR).
[analog I/O]	Bandwidth ADC Rates and Resolution DAC Rates and Resolution Clocking	6 channels at up to 80 MHz each 204.8 MSPS @ 12-bits, SFDR >68 dB 204.8 MSPS @ 14-bits, SFDR >60 dB Internal oscillators, locked to external 10 MHz reference input (reference not supplied)
[processing subsystem]	FPGA GPP	Twelve Xilinx® XC2V6000 Two Freescale MPC7410, four IBM 405GP embedded controllers
[external interfaces]	IF in IF out 10 MHz reference input Network interfaces RF Control interfaces	Six SMA Sockets, 50 Ohms, AC coupled Six SMA Sockets, 50 Ohms, AC coupled SMA socket, 50 ohms RJ45 copper interfaces: two 10/100, one 10/100/1000, one 1000 (Gigabit PMC) Two sets of 30 LVTTTL signals available at one D-sub37 and one D-sub50 connector
[platform requirements]	Operating System Tools	VxWorks 5.5.1 <i>quicComm</i> Software Development Kit (SDK), system examples
[development software]	Host Operating system FPGA tool chain	Microsoft Windows XP ISE Foundation
[electrical]	Supply Voltage (DC) Power Consumption	120/220 VAC at 50/60 Hz 1000 Watts typical
[mechanical]	Size	49 cm (height) x 48.5 cm (width) x 58 cm (depth)
[environmental]	Temperature RoHS	Operating temperature range of 0 to 50 degrees C Please see component level datasheets for RoHS compliance or contact Spectrum Sales
[ordering]	901-00022 901-00023	SDR-3002 EWDRP 11U 1st Development System SDR-3002 EWDRP 11U Recurring System
[availability]		60 day ARO