

SDR-3500 SMRDP

“Skinny” Military Communications (MILCOM) Rapid-Prototyping and Development Platform

cPCI



The only fully integrated COTS “RF to Ethernet” black-side solution comprising RF and single-slot modem hardware, together with all the software and tools necessary for rapid SCA compliant radio development.

Benefits

- Uses field-proven software defined radio technology
- Saves over 9 person-months of integration effort
- Supports multichannel radio development using a highly scalable and modular architecture
- Enables emulation of co-site interference
- Allows technology demonstrations in many airborne, maritime and fixed installation environments
- Highly customizable

Applications

Tactical Military Communications

- Rapid Prototyping
- Waveform Development
- Verification and Validation testing
- Beamforming and MIMO research

Features

- Supports one channel (scalable in increments of one) operating in full or half-duplex mode between 0.5 MHz and 3 GHz, with IF bandwidths of up to 30 MHz
- Based on Spectrum’s SDR-3000 family incorporating Xilinx® Virtex-4™ FPGA, Freescale MPC7410 PowerPC™ and TI TMS320C6416 DSP processing devices, all interconnected through high performance communications fabrics
- Support for both fast and slow hopping waveforms up to 5000 hops/sec
- Includes a comprehensive sample application with source code illustrating operation in a frequency agile environment
- GPS absolute time reference (IRIG-B and 10 MHz) with location
- Comprehensive training and support

Description

The SDR-3500 SMRDP¹ is a fully integrated, black-side software defined radio (SDR) platform providing a commercial off-the-shelf (COTS) “RF to Ethernet” radio platform for military communications programs. This platform offers the full modem processing functionality in a single slot, and can be considered a “skinny” version of Spectrum’s SDR-3000 MRDP. The SDR-3500 SMRDP integrates a high performance fast tuning transceiver with a Software Communications Architecture (SCA)-enabled signal processing platform that has been used for Joint Tactical Radio System (JTRS) waveform compliance testing. This integrated solution was designed specifically to de-risk customers’ programs by providing the fastest route to developing SCA-enabled architectures and systems, waveform applications, and verification and validation platforms. The solution includes resource-efficient programmable digital down-converter (DDC) and digital up-converter (DUC) FPGA cores and a system-level software example demonstrating the overall data flow. Source code for the examples and DDC/DUC cores is provided. The SDR-3500 SMRDP is at technology readiness level six for many fixed, airborne and maritime environments, making it suitable for field demonstrations and deployments.



Figure 1. SDR-3500 SMRDP components: SDR-3000 and DRT2110

¹ Subject to U.S. and Canadian export regulations.

Block Diagram

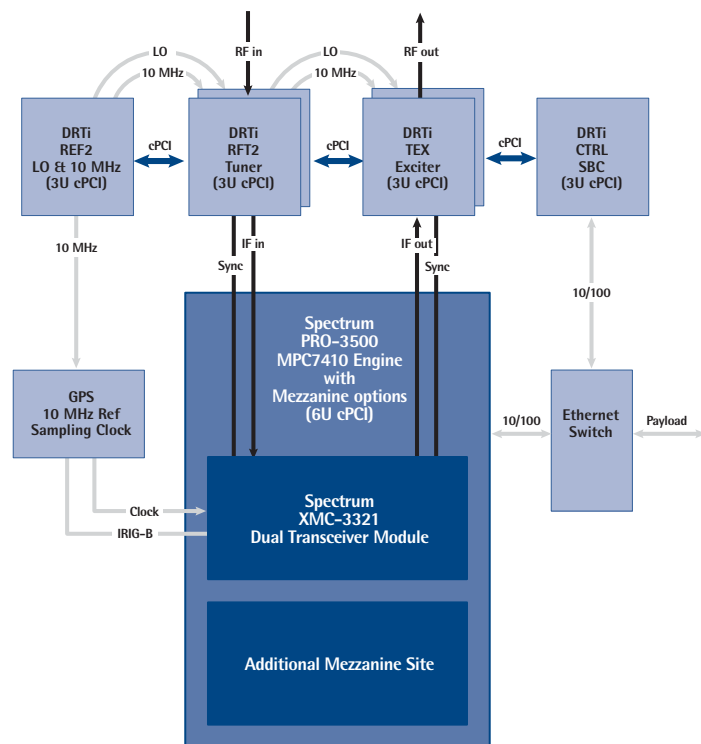


Figure 2. SDR-3500 SMRDP System Architecture

Architecture

The SDR-3500 SMRDP integrates a frequency agile RF transceiver subsystem, a high performance signal processing platform, and an SCA-enabled software operating environment into a scalable architecture for software defined radio applications.

[RF Transceiver Subsystem]

The RF transceiver subsystem consists of four basic elements from Digital Receiver Technologies, Inc., or DRTi (www.drty.com): an RFT2 tuner, a TEX exciter, a REF2 highly stable oscillator, and a DRT CTRL single board computer. A variety of packaging options are available including the DRT2110 Wideband Tuner System. This subsystem integrates the elements above into a single 20-slot 3U CompactPCI chassis.

For more information or to purchase the DRT2110 directly, please visit <http://www.drty.com>.

[Signal Processing Platform]

The SDR-3000 family of signal processing platforms was designed specifically for the requirements of software defined radio communications applications. It integrates heterogeneous processing elements (FPGAs, DSPs, and GPPs) seamlessly using a high performance embedded fabric. The SDR-3500 SMRDP uses Spectrum's XMC-3321 wideband analog I/O mezzanine module sitting upon the PRO-3500 baseband processing engine to provide a single-slot modem solution. Due to its modularity, the platform can also evolve with your future needs as Spectrum continues to expand its XMC-based I/O offering. More details on the SDR-3000 family can be found at www.spectrumsignal.com/products/sdr.

Software

In addition to the base software layers (Spectrum's *quicComm* and SCA BSP) offered in the RF subsystem and the SDR-3000 platform, the SDR-3500 SMRDP provides other valuable software and FPGA core functionality:

- The Harris dmTK, an SCA core framework and development toolset, fully integrated onto the SDR-3000 platform
 - Optimized, programmable digital down converter (DDC) and digital up converter (DUC) FPGA cores interfacing to the IF (see Figure 3)
 - Fully programmable FIR coefficients on up/down converters
 - Capability to downconvert multiple channels from same digital IF (optional)
 - Highly resource-efficient cores due to serialized implementation
 - Support for time sensitive and time slotted applications through:
 - Time stamping of ADC input samples
 - Time triggering of DAC output samples
 - An RF control API to manage all functionality of the RF subsystem
 - A comprehensive data flow example from the RF input, through the entire signal processing chain, and back out the RF output
- Source code for the RF control, hopping, DDC/DUC cores and time stamping is provided as part of the platform.

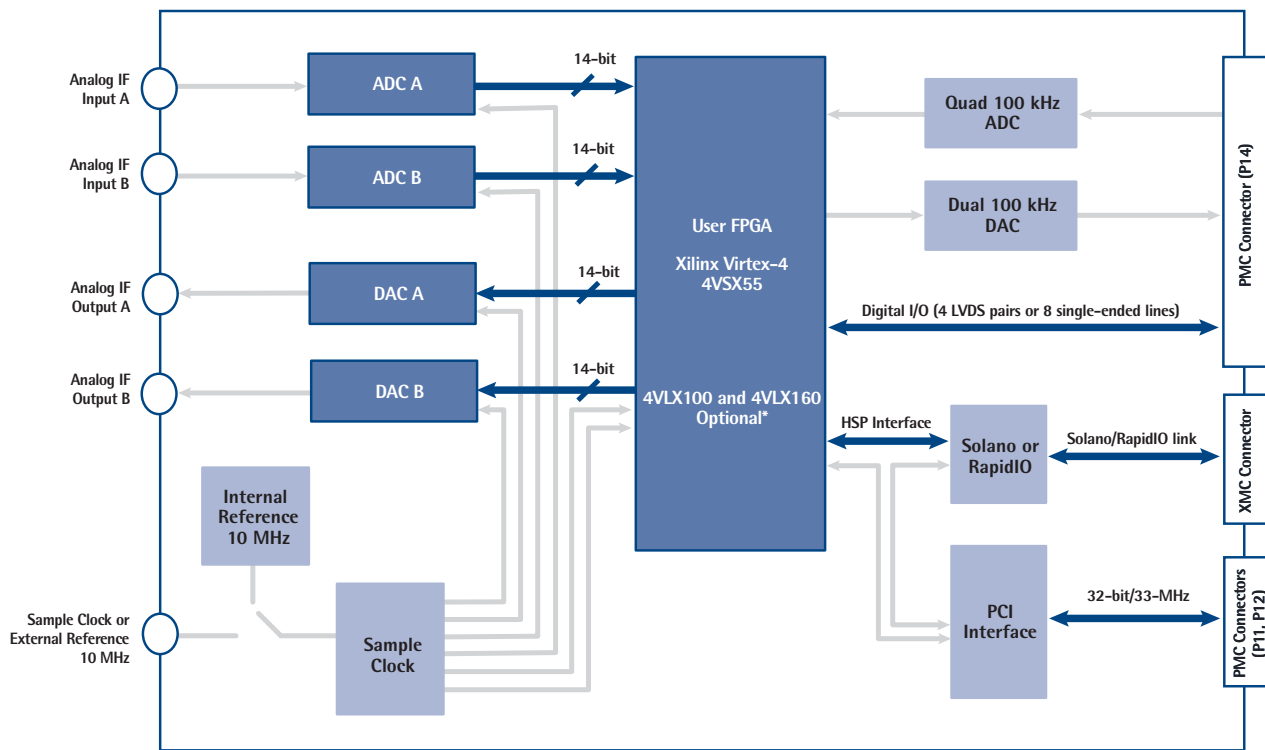


Figure 3. XMC-3321 dual transceiver block diagram

Operation

The RF subsystem is capable of being controlled using two methods: front panel Ethernet and SMA synchronization signals. A sockets-based control library running on a PowerPC communicates over the Ethernet interface to the CTRL single board computer in the RF subsystem box. Frequency and attenuation commands are written and status is queried over this interface. In addition frequency tables may be loaded onto the TEX and RFT2. The Tuner and Exciter Sync signals allow for low latency and deterministic stepping through these frequency tables. Fine tuning of the frequency setting is achieved through a combination of coarse tuning of the RF subsystem and fine tuning of DDC and DUC cores on the FPGA processor. IF data flows through the FPGA processor allowing for precise control of data burst insertion or acquisition.

The system is designed to update the frequency table continuously in real-time. GPS absolute time via IRIG-B and 10 MHz reference are available and can be used to time stamp the incoming packets or to schedule outgoing packets. In addition, the system can be synchronized with external devices using optional External Syncs.

Customization

The supplied example application, including source code, shows the capability of the Radio System. Spectrum's Application Engineering Services (AES) team will help you map your application requirements to the platform and tailor the platform to your specific needs. In addition, the team's SCA expertise and application software/firmware components can be employed to speed your time to deployment.

In addition, Spectrum's Application Engineering Services team in Columbia, Maryland, USA can customize the SDR-3500 SMRDP to modify existing or add additional features as required, such as:

- QPSK Mod & Demod
- TDM processing
- Polyphase resampling
- Channelization
- FSK Mod & Demod
- Frequency Hopping
- FFT

Specifications

[export regulations]		The SDR-3500 SMRDP is subject to the export control laws of the United States including the United States International Traffic in Arms Regulations (ITAR).
[general]	RF Subsystem Processing Subsystem GPS	DRT2110 Spectrum SDR-3000 (PRO-3500, XMC-3321) FEI Zyfer GPStarPlus (subject to change)
[analog I/O]	Recv IF Sample Rate Xmit IF Sample Rate	up to 213.33 MSPS at 12 bits up to 213.33 MSPS at 14 bits
[RF subsystem]	Rx RF Frequency Tx RF frequency Rx IF Band Tx IF Bandwidth Xmit Freq Table Size Recv Freq Table Size	0.5 MHz to 3 GHz 40 MHz to 2.9 GHz 30 MHz 30 MHz Up to 500,000 Entries Up to 500,000 Entries
[processing subsystem]	FPGA GPP DSP	Xilinx 4VLX160 Two MPC7410 (more are optional), one IBM405 (more are optional) Optional Texas Instruments TMS320C6416 (two or four)
[external interfaces]	Rx Tuning Sync Tx Tuning Sync External Sync Ethernet RF Channels Absolute Time	5000 hops/sec (limited by RF receiver) 5000 hops/sec (limited by RF transmitter) LVTTL 10/100 BT Up to two receive and one transmit channel, operating in full or half-duplex mode IRIG-B
[development software]	Operating System CORBA SCA Core Framework	Wind River VxWorks V5.5.1 OCI TAO v1.3a Harris dmTk v2.3 (SCA 3.0 compatible)
[environmental]	RoHS	Please see component level datasheets for RoHS compliance or contact Spectrum Sales
[ordering information]	901-00045 901-00046	SDR-3500 SMRDP RECURRING PRODUCTION SYSTEM* SDR-3500 SMRDP 1ST DEVEL MENT SYSTEM* Note: To order the DRT2110, please contact DRTI directly at www.drty.com