

Benefits

- Dynamically reconfigurable, high performance parallel processing engine
- Supports implementation of multi-channel, multi-mode receivers for both narrowband and wideband air-interfaces
- *quicComm*[™] software architecture accelerates application development, simplifies the programming model and ensures code portability
- Deterministic operation; the time taken to process and move data is guaranteed

Applications

- Signals Intelligence (Wideband Spectral Analysis, Multi-channel Direction Finding)
- Electronic Support (SIGINT on the battlefield)
- Surveillance RADAR
- Tactical & Satellite Military Communications (MILCOM and MILSATCOM)

Features

- Single-width XMC form factor
- Conduction* and air-cooled versions
- High speed, low latency deterministic data paths to processing engines provided over XMC interface by Solano Technology. Parallel RapidIO[™] (VITA 42.1) is a future option*.
- User-programmable Xilinx[®] Virtex-4[™] LX160 FPGA device (LX40 up to LX100 and SX55 are future options*)
- Two banks of 512MB DDR2 SDRAM totaling 1 GB
- 32-bit/33 MHz PCI bus interface for control
- JTAG connector compatible with Xilinx's ChipScope[™] debugger
- Modular front panel I/O interface to granddaughter cards that support a variety of I/O formats (air-cooled module only)

Description

The XMC-8131 is a key component in Spectrum's series of software defined digital radio modules from the *flexComm*[™] wireless communications product line. The XMC-8131, a single-width XMC (VITA 42.0) module, is intended for use as a front-end signal processing engine, or a general-purpose fixed-point or floating-point co-processor with a modular front panel interface to support a variety of I/O formats. The XMC standard is fully compatible with IEEE P1386.1 PMC standard but offers the additional benefit of dedicated high-speed links between an XMC-compliant mezzanine and carrier cards.

The XMC-8131 incorporates a single programmable Xilinx[®] Virtex-4 FPGA device. The standard configuration comes with the LX160 supporting 152,064 logic cells (LX40 up to LX100 and SX55 are future options*). A second Xilinx Virtex-4 FPGA is used to offload the communications to the carrier board from the user parts. This high-speed communications can be done via four low power Solano Communication IC compatible links or a dual Parallel RapidIO industry standard VITA 42.1 connection*. The module features two banks of DDR2 SDRAM totaling 1 GB of capacity.



* See future options section of this datasheet.

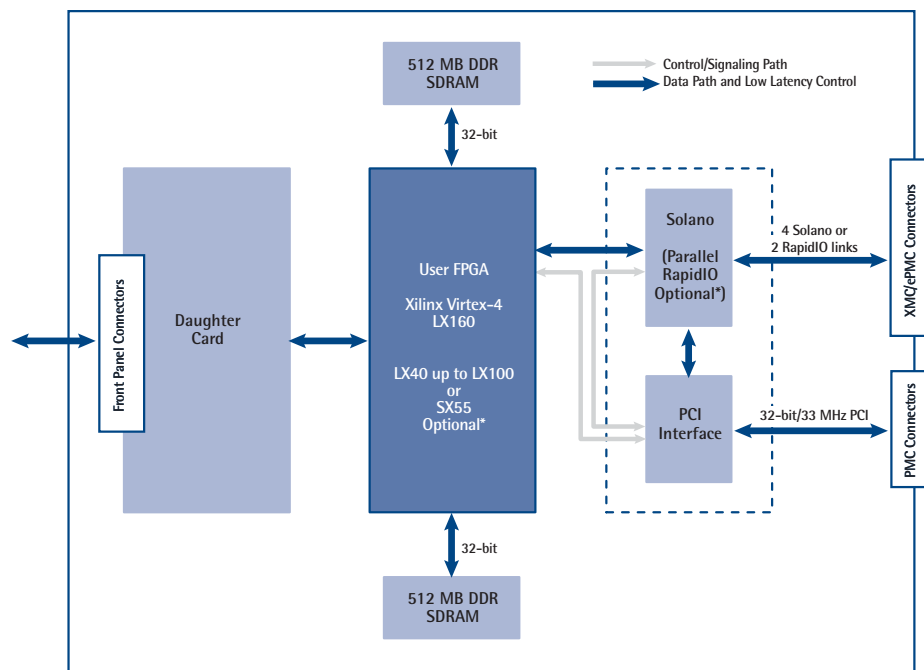


Figure 1. XMC-8131 Block Diagram

Architecture

[Solano Communications Technology]

The XMC-8131 supports four Solano Enhanced PMC (ePMC) links via the XMC interface. The Solano Communications Technology used in the ePMC specification provides high bandwidth deterministic data paths between ePMC mezzanine modules and ePMC carriers. Each Solano high-speed link is capable of greater than 200 MB/s full-duplex communications. Solano provides the benefit of low power consumption for applications operating under a constrained power budget.

[XMC and Parallel RapidIO* Compatibility]

The VITA 42.0 XMC mezzanine card base standard defines physical features that enable switched communications between a standard mezzanine card and its carrier. The XMC-8131 supports an optional dual Parallel RapidIO link that is capable of low latency deterministic operation and interface to industry standard XMC-compliant carrier cards.

The VITA 42.1 Parallel RapidIO standard uses a point-to-point scalable switched-fabric for its transport layer. Using LVDS signaling with a double-data-rate clocking methodology, link rates per bit line of up to 500 MB/s are supported (please see future options).

[Xilinx Virtex-4 FPGA]

The Xilinx Virtex-4 FPGA platform is ideally suited for high-performance signal processing tasks. On the XMC-8131, a Xilinx Virtex-4 (LX160) is available for user programming (LX40 to LX100 or SX55 are future options*). Power consumption of the Xilinx Virtex-4 is reduced by approximately 50% over comparable Virtex-II Pro™ FPGAs using Xilinx's Triple-Oxide Technology. Resources available on the LX and SX parts are as follows:

Device	4VLX160	4VLX40*	4VLX60*	4VLX80*	4VLX100*	4VSX55*
Logic cells	152,064	41,472	59,904	80,640	110,592	55,296
Block RAM (Kbits)	5,184	1,728	2,880	3,600	4,320	5,760
18 x 18 Multipliers	96	64	64	80	96	512
Digital Clock Management Blocks	12	8	8	12	12	8

* See future options section of this datasheet.

[Interfaces]

The XMC-8131 uses a standard Spectrum daughter card to provide a modular I/O front-panel interface (air-cooled version only) supporting access in a variety of formats such as:

- 4 IF input Low Voltage Differential Signaling (LVDS)
- 4 IF output LVDS
- 2 IF in / 2 IF out LVDS
- LVTTTL

For example, the 4 IF input LVDS daughter card has a synchronization connector available to allow multiple modules to maintain synchronous operation for coherent applications such as beam forming and direction finding. In this configuration, the XMC-8131 is capable of receiving up to four 80 MSPS digital IF (intermediate frequency) channels via the front panel.

The XMC-8131 is compatible with carrier boards that support XMC/ePMC connectivity, equipping users with a powerful versatile module that is suitable for a wide variety of applications.

Software

[*quicComm* Software Development Kit (SDK)]

The XMC-8131 software interface is via a *quicComm* SDK that is available on all supported platforms. *quicComm* software equips users with basic link level access and control of Spectrum's *flexComm* products and significantly accelerates user application development. It is also standard across all *flexComm* products, allowing code portability. This software includes a board support package for control and data handling which:

- Allows configuration and control of the data links between processors and mezzanine cards
- Initiates and manages data transfers
- Enables dynamic loading on a processor without affecting other processors

As a part of Spectrum's *quicComm* package, an FPGA wrapper is provided to abstract all board level interfaces on the Virtex-4 FPGA, including the interfaces to the memory, daughter card, communication fabrics and control. The wrapper is designed so users can expedite the integration of third party or custom FPGA IP cores into the XMC-8131 module.

[Xilinx ISE Foundation™]

ISE Foundation is the integrated programmable logic design environment recommended for FPGA development on the XMC-8131. It includes: schematic capture, power analysis tools, physical synthesis for FPGAs, advanced Place and Route Algorithms, HDL Advisors and Timing Cross-Probing. It also contains COREgenerator, a graphical interactive design entry tool used to create high-level modules. COREgenerator gives access to a library of hundreds of FPGA IP cores, many of them free, from Xilinx and third-party vendors. This library includes DSP applications such as digital down converters (DDC), direct digital synthesizers (DDS), FIR filters, FFT, numerically controlled oscillator (NCO), memory controller and many others.

[RF Engines]

RF Engines Ltd. (www.rfel.com) provides individual IP cores and integrated turnkey designs for digital RF signal processing in FPGAs and ASICs as appropriate to speed development. RF Engines provides off the shelf IP cores that are highly optimized in terms of speed, power and size compared to cores available from the major FPGA vendors. RF Engines' FPGA IP available cores include: pipelined FFT, tunable PFT, halfband filters, highly optimized FIR filters, windowing and CORDICS.

For application specific requirements, Spectrum can develop custom cores when these are otherwise unavailable. If you have such a requirement, please contact Spectrum Sales.

Specifications

[general]	FPGA Device RAM	Xilinx Virtex-4 XC4VLX160 (-12 speed grade) Two banks of DDR2 SDRAM, each with 512 MB and a 32 bit interface at 200 MHz
[external interfaces]	Link IF PMC Host JTAG Connection XMC Interface ePMC Interface	Input/Output, 48-bit LVDS high-speed user-changeable GPIO front-panel interface PCI bus 32-bit/33 MHz PCI interface following IEEE P1386.1 specification JTAG connector for Virtex-4 FPGA, Xilinx ChipScope™ debugger compatible Four Spectrum Solano~links, each providing greater than 200 MB/s (full-duplex) Four Spectrum Solano~links, each providing greater than 200 MB/s (full-duplex) - uses XMC connector
[compatibility]	Supported Carriers Operating System	PRO-1900/PRO-1901 Refer to carrier specifications
[development software]	Application Libraries FPGA Code Development HDL coding language	<i>quicComm</i> Software Development Kit ISE Foundation tools from Xilinx and ModelSim® PE from Model Technology are required, Synplify Synthesis® from Synplicity is recommended VHDL
[electrical]	Supply Voltage (DC) Power Dissipation	Supply Voltage +5V, 3.3V +5%/-3% (supplied by PMC connector) 4 - 16 watts depending on FPGA and SDRAM utilization
[environmental]	Operating Temperature Storage Temperature Humidity RoHS	FPGA @ 6 watts Air-cooled: Operating temperature range of 0 to 55° C per VITA47 EAC1 -50 to +100° C 10% to 95% relative humidity, non-condensing 5 of 6 compliant (Pb solder exemption). For RoHS ordering information, other RoHS compliance options or certificates of compliance, please contact Spectrum Sales.
[ordering information]	650-00145	XMC-8131-CAC-LX160-12 + ICM FOR EPMC SITES
[future options]	FPGA Device PMC Host XMC Interface Carriers Extended Temperature	Future options may be implemented at the discretion of Vecima Networks Inc. or its subsidiaries based on market demand.** LX40/60/80/100, V4SX55 PCI bus 32-bit/66 MHz PCI interface Two optional Parallel RapidIO link providing 500 MB/s (full-duplex) PRO-2900, PRO-3500, PRO-4600 Conduction-cooled: -40 to +70° C card edge per VITA47 ECC3 (available only with -11 or lower FPGA speed grade)