

Multi-Channel Direction Finding System

Authored by Cyrus Sy, Field Application Engineer
Spectrum Signal Processing



Application Note

Introduction

Direction finding (DF) is a term used to describe the process of locating, tracking and distinguishing various sources of radio transmissions. DF is a well-established technology, and has become increasingly popular in military and commercial communications.

DF systems calculate the direction of arrival of a particular radio signal using an array of spatially displaced antennas or rotating antenna. Nearly all DF algorithms require that signals from multiple antennas are received and routed to multiple processors or DSPs. These processors or DSPs are then used to compare the phase and arrival time from the various signals to derive the location, speed and direction of the signal source.

This application note describes how Spectrum helped one particular customer to develop a high performance DF system, with the following requirements:

- › Direction finding in the HF frequency range (1.5-30 MHz)
- › Twelve antenna elements
- › Overall control of system via a single board computer
- › Ability to remotely control the system via TCP/IP over an Ethernet LAN

This application presented several challenges for the customer. One of the challenges of this particular DF system was the requirement for coherent sampling of 12 antenna inputs. All DF algorithms require coherent ADC sampling of all input signals so that phase information is not lost. The second challenge was the complex data flow required between the A/D and processors, as well as between the processors themselves. Figure 1 illustrates the signal flow of the customer's DF system. First, blocks of samples were digitized, where the block size is a run time programmable parameter. Samples were then sent to a processor where a fast fourier transform (FFT) was applied (front end processing). FFT results from one processor then were distributed to all the other processors for comparison and further calculation (backend processing). Final results were then sent to the host SBC from where they were transmitted across the TCP/IP network for further non-real-time processing.

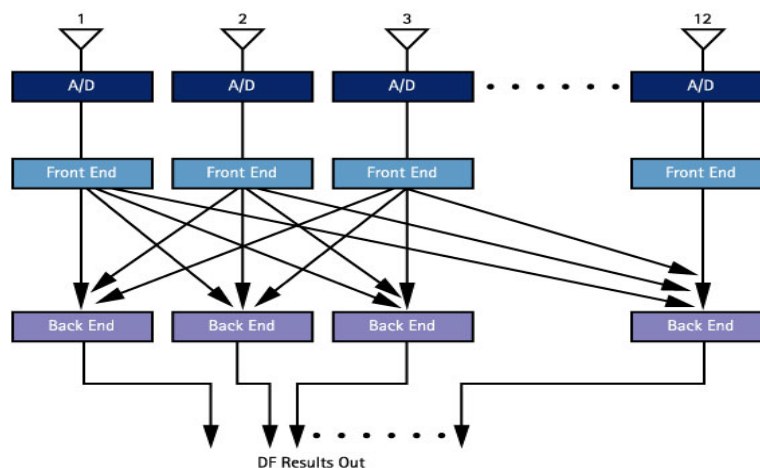


Figure 1: High Level Signal Flow for Direction Finding System

A third challenge was the customer's requirement for additional pre-processing of the raw digitized data before undergoing an FFT by the processors. The raw data had to be filtered, decimated, and run through threshold level monitors.

Spectrum's flexComm HCDR-100x-based subsystems are well suited for applications such as this one that require scaleable, high-bandwidth inter-processor and inter-board communications, in addition to modular I/O. The Spectrum solution consisted of the ePMC-PPC, dual G4 PowerPC processing engine, and the ePMC-2ADC, a dual channel A/D converter, both of which are mounted on the PRO-1900 PowerPC intelligent carrier board. Since this configuration gives us two antenna inputs per VME slot, we scaled the system to 12 channels by using a total of 6 PRO-1900 boards with PowerPC and A/D modules (see Figure 2).

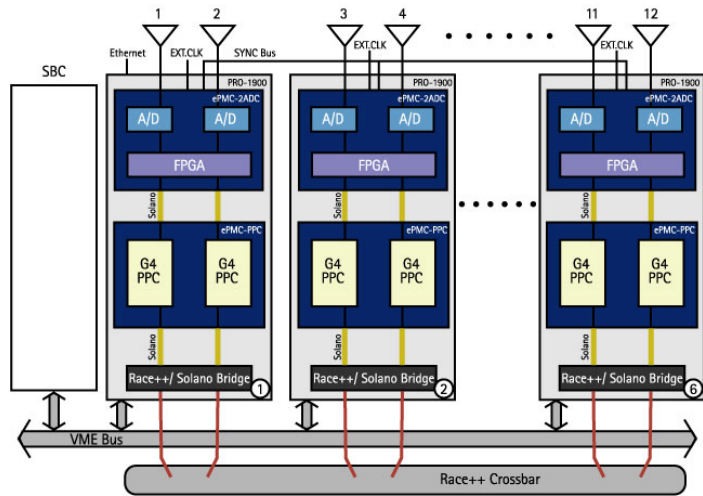


Figure 2: Race++ Based DF System using Pro-1900; ePMC-PPC and ePMC-2ADC

Given the configuration in Figure 2, Spectrum was able to overcome the challenges presented in the following ways:

Coherent Sampling of 12 A/D Converters

The ePMC-2ADC features both an external clock input and a software-enabled external synchronization bus (sync I/O). The sync I/O interface allows one master ePMC-2ADC to synchronously initiate sampling on the other five slave ePMC-2ADCs by using a six drop locking ribbon I/O connector. All of the ePMC-2ADCs share the same clock source at the desired sampling frequency.

System Data Flow for DF Algorithm

Two antenna inputs are sampled synchronously by the ePMC-2ADCs by a common clock source. Digitized samples are sent through an on-board FPGA for pre-processing, and into the PowerPC via Solano-links, each capable of 200 MB/s full-duplex of bandwidth. The PowerPCs compute the FFT, and the results are then broadcast to the other PowerPC processors on the other PRO-1900 boards, via Race++ which provides point-to-point data links between boards at up to 200 MB/s full-duplex each link. The end results of the DF calculations are written to the single board computer via the VME bus. Through the use of the embedded processor on the PRO-1900, onboard DMA controllers, and high-speed interfaces such as Solano Communications IC and Race++, data can be transferred in and out of the processors without burdening them in the actual transfer and without missing samples.

Pre-Processing of Raw IF Data Stream

Spectrum's ePMC-2ADC features a Xilinx Virtex XCV300E FPGA that is designed specifically for IF pre-processing. Using our in-house FPGA application expertise, our engineers wrote customized firmware to implement the filtering, sample-stream decimation, and threshold functions. Spectrum's extensive use of FPGAs led to an extremely flexible and re-configurable architecture. Distributing the IF processing among FPGAs and PowerPCs, combined with the use of high bandwidth, low-latency data links such as the Solano Communications IC and Race++, maximized the total processing and data throughput performance for the customer. By providing a fully integrated solution, the customer was able to quickly begin development on a system that would meet their application performance requirements.



Wireless Systems

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