

Facilitating Technology Insertion in Advanced Wireless Systems

Part 2: Real-World Examples

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Part 1 of this article proposed an architectural model facilitating technology insertion of intermediate frequency and baseband or modem processing engines in advanced wireless systems. These subsystems often include a variety of programmable “off-the-shelf” signal processing devices such as digital signal processors (DSPs) and field programmable gate arrays (FPGAs) which tend to evolve following some variant of Moore’s Law, with new generations of devices incorporating new features and capabilities introduced every 2 to 3 years. Original equipment manufacturers (OEMs) developing advanced wireless systems can often take advantage of this trend to offer their customers competitive feature enhancements and upgrades of existing systems through technology insertion. This is a cost-effective method of introducing new features by replacing only the baseband processing engine while retaining other subsystems, such as the RF or control subsystems, as is.

The model proposed for supporting this capability starts by encapsulating the baseband processing engine in a “standardized” modular architecture. The term “standardized” in this context means having a well-defined mechanical structure or form factor that can facilitate the future replacement of the baseband processing engine while the system is in-service and having well defined interfaces between the baseband processing module and the other subsystems within the radio, including the mechanical and electrical interfaces and associated intra-system communications protocols. The model further proposes that, in addition to “standardizing” the form factor and interfaces, support for technology insertion also requires establishing a well-defined operating environment within the baseband processing engine to facilitate reuse of the functional code supporting the physical layer processing. The reason for such an environment in supporting technology insertion is simple: significant reductions in both cost of development and time to market can be achieved by the OEM if, for example, the DSP code in one generation of baseband processing engine can be largely reused to support the same or similar functionality in the next.

Part 2 of this article examines the proposed architecture further by exploring the efficacy of the proposed model in two real world examples – a wideband receiver platform, and a tactical military communications technology demonstrator platform.

Case Study 1 – Wideband Receiver Platform

The Problem

In this case study, a radio system original equipment manufacturer (OEM) was pursuing multiple different programs where they needed the ability to monitor the spectrum over a wide frequency range and extract signals of interest for follow-on processing. The signal

processing architecture of the OEM's system included three primary subsystems, as illustrated in Figure 1:

- The Spectral Analysis Subsystem, which performs a spectral analysis on the digitized wideband signal to detect potential signals of interest. This processing was primarily performed in an FPGA.
- The Channelization Subsystem, which buffers the received signal until a signal of interest is detected and then extracts signals of interest from the wideband signal and converts them to baseband for channel processing. Process to support signal extraction is performed primarily in an FPGA, whereas channel processing is primarily performed in a DSP or general purpose processor (GPP).
- The Operational Control Subsystem, which provides overall "real-time" control of the wideband receiver system while in operation.

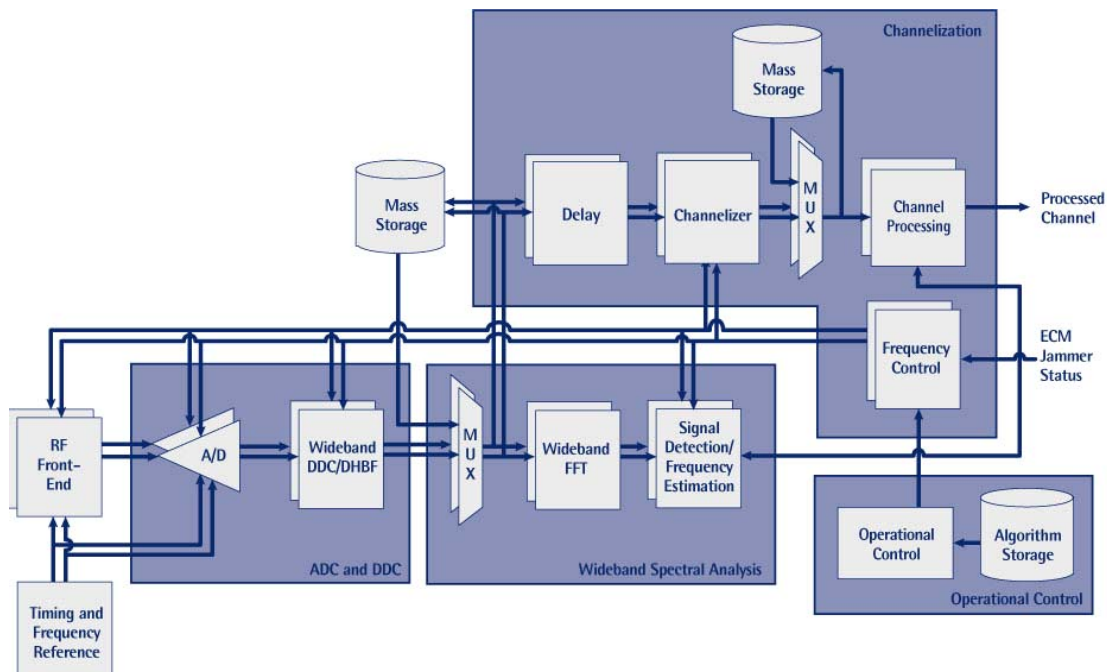


Figure 1: High Level Architecture of the OEM's Wideband Receiver System

The OEM had three key problems in developing and fielding this type of system. First, the number and types of channels required in the wideband receiver architecture varied from program to program based on each program's specific requirements. Given the tight time constraints generally associated with their programs, the OEM needed an architecture that allowed them to easily mix and match the number and types of FPGA and DSP processors used within one system without the need to design new hardware for each program. Secondly, the OEM planned to invest heavily in the development of the FPGA and DSP application code for their initial programs, and then reuse this intellectual property (IP) as a critical differentiator in winning future programs. To maximize their return on investment in this IP, the system architecture had to maximize reuse of the IP from program to program. Finally, the OEM's customers required the ability to minimize the effort, cost and disruption associated with adding enhanced features, capabilities and

processing power to existing systems. Expensive forklift upgrades of the existing systems were not an option.

The Solution

To solve these problems, the OEM used an “off-the-shelf” signal processing platform which supported modularized IF and baseband signal processing technologies that could be mixed and matched to meet with each individual program’s specific needs. The platform selected was the HCDR-1000 subsystem by Spectrum Signal Processing By Vecima (see Figure 2). Each FPGA or DSP processor provided in this platform is encapsulated as an independent processing node: integrating a processing device, one or more peripheral devices such as memory, and input/output data communications fabric interfaces all onto a standardized modular form factor. The communications fabrics supported on this platform, when coupled with the platform’s software operating environment, facilitate deterministic, low latency “any to any” communication between processing nodes, allowing the OEM to create a tailored wideband receiver architecture for each of their target programs by mixing and matching FPGA and DSP modules as necessary following a common platform model.

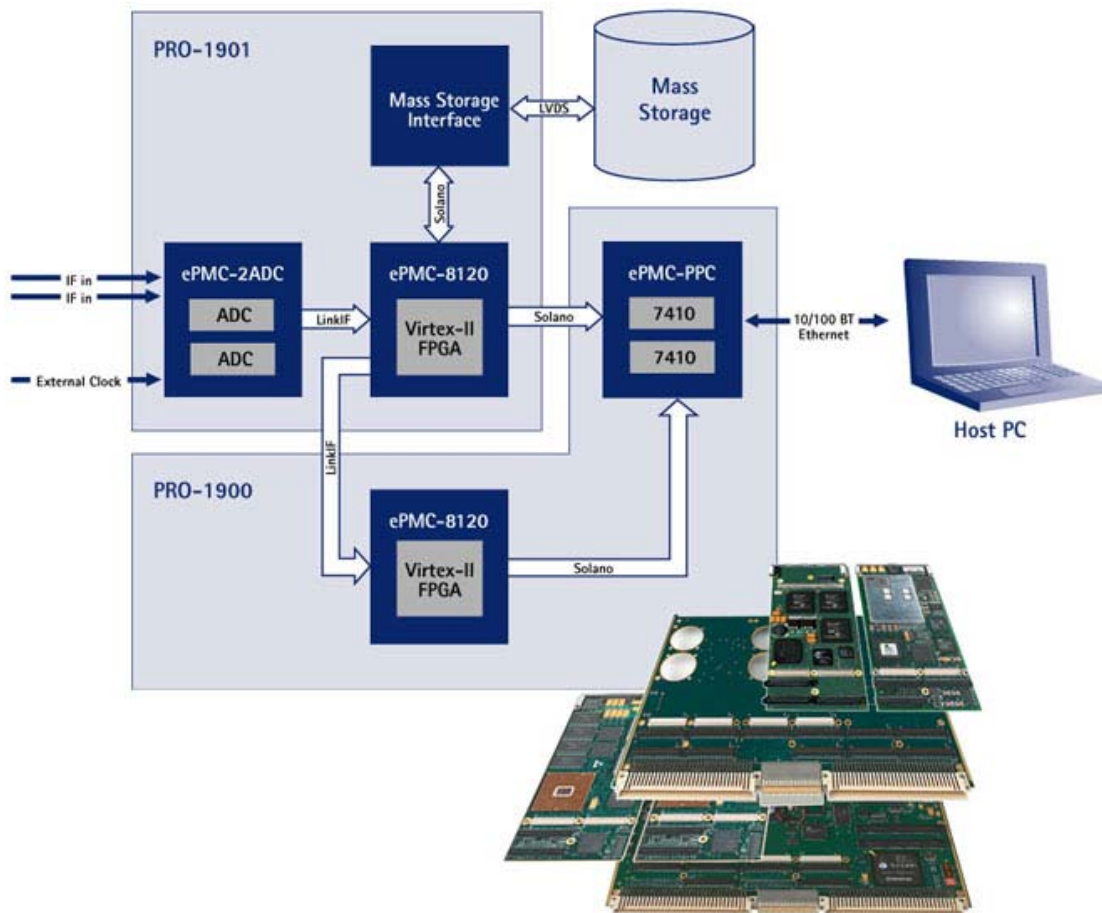


Figure 2: IF and Baseband Processing Architecture for a Wideband Receiver System Based on HCDR-1000 Technology

The use of standardized modules in the HCDR-1000 platform also allowed the OEM to provide upgrades to each wideband receiver system while it was in service by simply replacing processing modules as new technologies became available (See Figure 3). The HCDR-1000 software operating environment includes a hardware abstraction layer, known as *quicComm*[™]. This abstraction layer is consistent across each generation of the product, and enabled to the OEM to reuse its code application with each system upgrade.

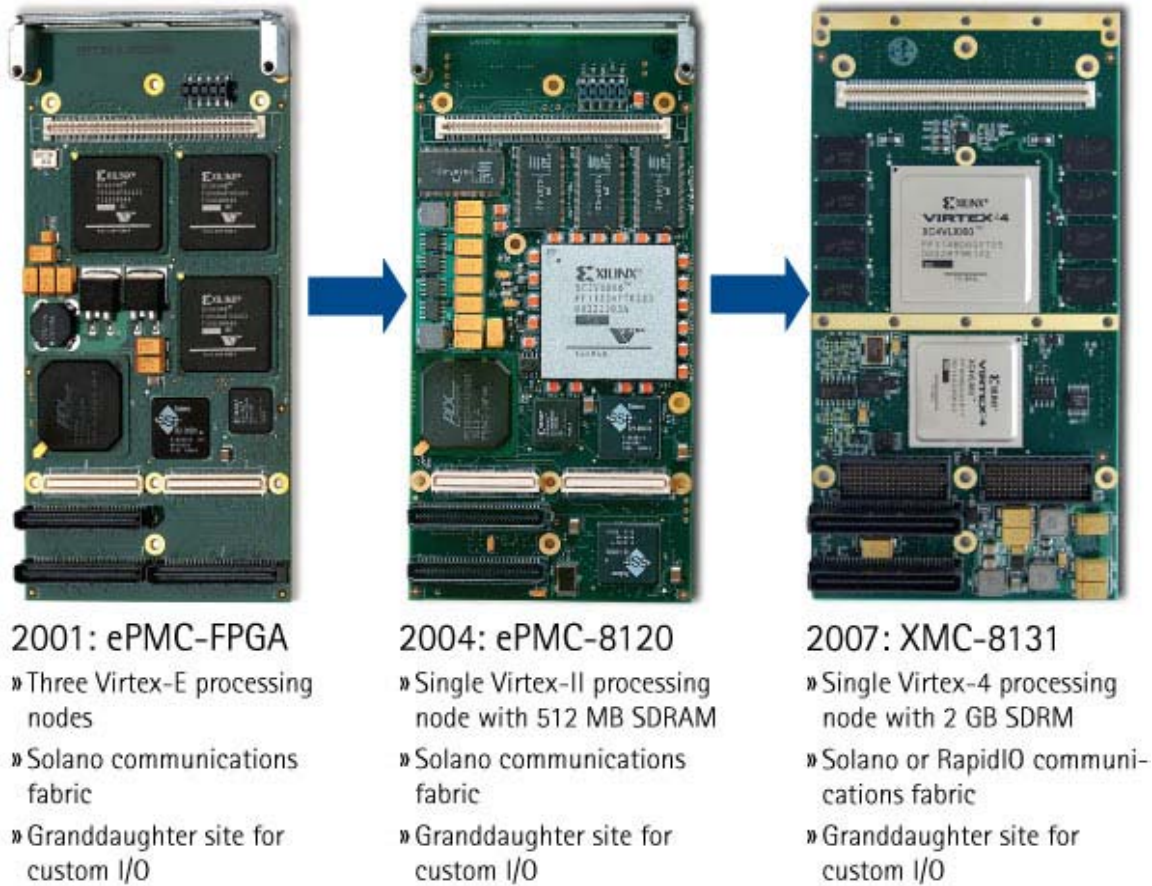


Figure 3: Evolution of FPGA Processing Node Over Six Years in the HCDR-1000 Platform

The Result

By utilizing a modular platform such as the HCDR-1000, the OEM was able to bring new wideband receiver technologies to their customers quicker than their competition who often required a ground-up development for each new program. In addition, the ability to reuse much of their application code from program to program reduced their overall cost, providing a further competitive advantage. These advantages, when coupled with the ability to more easily support their customers with new features and capabilities over the life of each fielded wideband receiver solutions allowed the OEM to pursue and win a multitude of new programs.

Case Study 2 – Tactical Military Communications (MILCOM) Technology Demonstrator Platform

The Problem

A General Dynamics Canada (GD Canada) development team was tasked with developing and demonstrating a software defined radio (SDR) that could support the future tactical communications needs of Canadian Forces. The SDR demonstrator had to support two legacy waveforms, one analog and one digital. To support this demonstration effort, GD Canada selected the high-performance SDR-3000 platform from Spectrum Signal Processing by Vecima, to simplify their waveform development and allow them to get to their initial demonstration quickly. This platform, illustrated in Figure 4, provided a host of high-end IF and baseband signal processing resources that included:

- Two Freescale™ MPC7410 GPPs,
- Four Xilinx® Virtex™-II FPGA processors, each with 128 MB of SDRAM,
- Four independent analog to digital converters (ADCs) and digital to analog converters (DACs) suitable for generation and reception of signals at standard military IF frequencies, and
- Spectrum's *flexFabric* digital links facilitating high-speed signal transfer between the GPPs, FPGAs, DACs, and ADCs.

The GPPs contained within the SDR-3000 platform used the VxWorks Real-Time Operating System (RTOS) by Wind River. Spectrum provided board support packages and its *quicComm* hardware abstraction library, which allowed the GPP to control hardware features such as *flexFabric*. Spectrum also provided firmware wrapper files for the FPGA board that acted as an extension to *quicComm* and allowed the user FPGA application to interface with hardware resources, including *flexFabric*.

As part of the SDR development program, GD Canada developed the application firmware to modulate and demodulate the selected waveforms. Additional firmware was written to configure the system and send/receive data over Ethernet. A digital upconverter (DUC) and digital downconverter (DDC) were required to convert between baseband and intermediate frequency signals. These were implemented as FPGA applications.

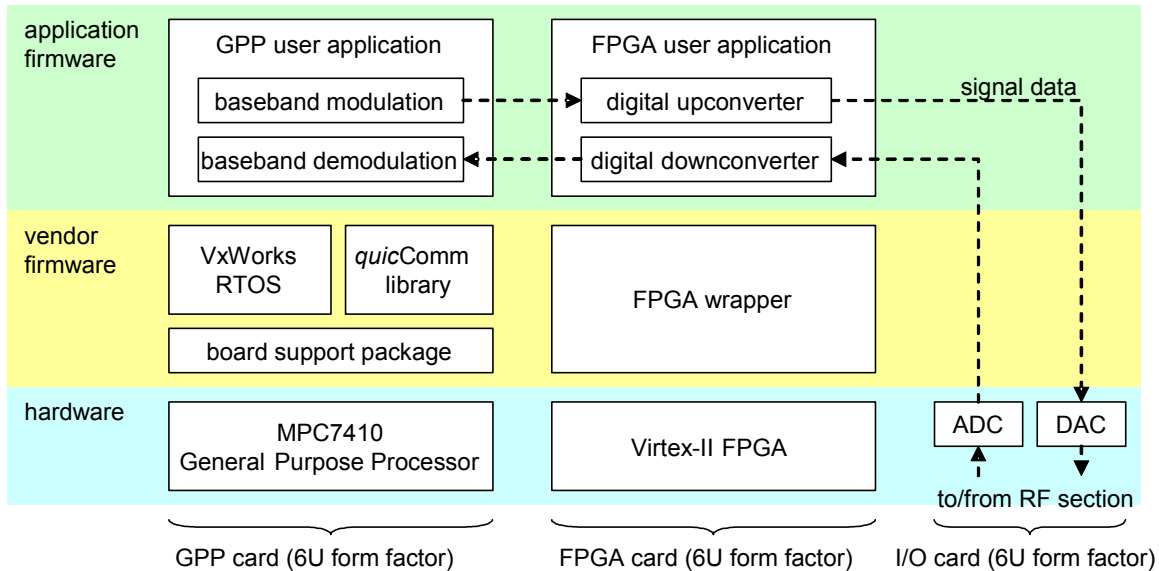


Figure 4: Architecture of Original Digital Subsystem for the Tactical Military Communications Technology Demonstration

While the abundance of resources available in the SDR-3000 platform simplified development and demonstration of SDR capability in a lab environment, the system was designed for deployment in fixed or semi fixed infrastructure locations, such as a network operating center or mobile command center, and as such it was unsuitable for demonstrating the technology to Canadian Forces in a highly mobile field environment. These environments impose severe constraints on size, weight and power, and require significant levels of ruggedization to accommodate the often harsh environment. In addition, the SDR-3000 platform was designed to support multiple concurrent channels of operation, versus the single channel per system operation inherent in most tactical military radios, making the cost of the SDR-3000 platform disproportionately high to support the target waveforms as a deployed tactical radio system. GD Canada needed to implement the same SDR capability on a compact, rugged platform that was better optimized for cost and power efficiency. The challenge in doing this was to maximize re-use of code that was developed on the original SDR-3000 based technology demonstrator platform and to minimize the porting costs associated with replacing the SDR-3000 platform in their overall demonstration system.

The Solution

The solution to this problem was to migrate the waveform application code to a new hardware architecture, Spectrum's SDR-4000 Wireless Modem (WM) platform illustrated in Figure 5. The new hardware was much smaller in size (3U form factor) with a reduced set of resources that included:

- a single Freescale MPC8541E GPP,
- a single Xilinx Virtex-4 FPGA, and
- dual ADC and DAC for analog I/O.



Figure 5. Spectrum's SDR-4000 Wireless Modem (WM)

Despite differences between the processing components used on the SDR-3000 and SDR-4000, both systems employed the same signal chain from a high-level perspective (GPP, FPGA, ADC and DAC), and as with the SDR-3000 platform, resources on the SDR-4000 were also interconnected through Spectrum's *flexFabric* links. At the time the project was started, the VxWorks operating system was not available for the new GPP card so it was necessary for GD Canada to switch to the INTEGRITY® RTOS from Green Hills® Software, Inc. This resulted in a change in the development tools for the GPP firmware. Spectrum provided the required board support packages, the *quicComm* hardware abstraction library, and the wrappers for the FPGA. The application firmware for the new system had the same functional requirements as before, with the GPP providing baseband modulation, baseband demodulation, Ethernet communications, and system configuration, and the FPGA providing DUC and DDC functionality.

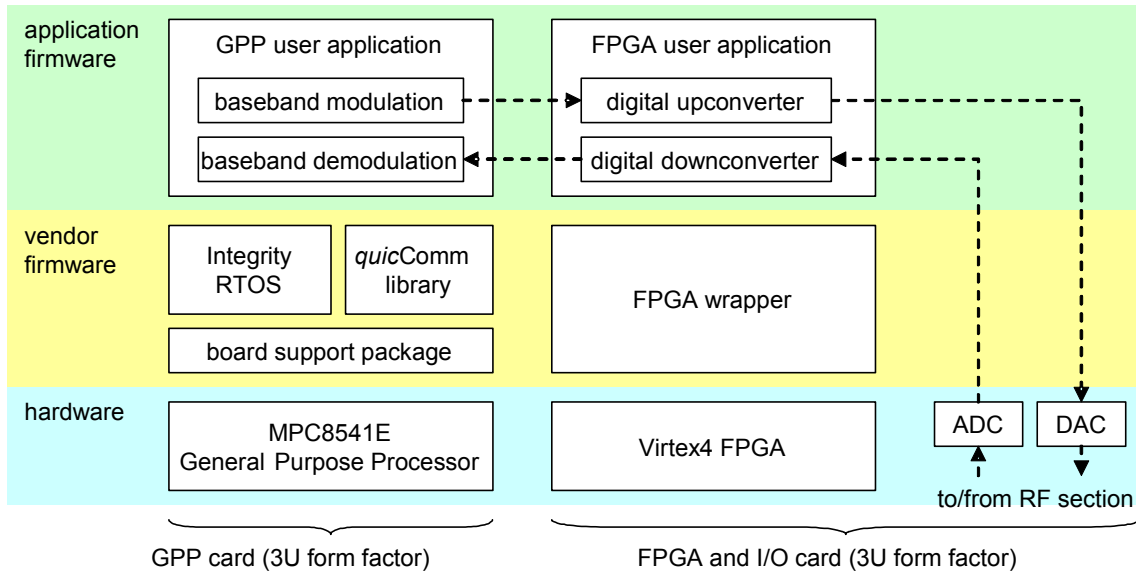


Figure 6: New Digital Subsystem for the Tactical Military Communications Technology Demonstration

The first step in the transition effort to port the application from the SDR-3000 to the SDR-4000 was to install the development tools for the new RTOS and FPGA. This included the MULTI development environment for Green Hills INTEGRITY and a new version of Xilinx ISE to support the Virtex-4 FPGA with its accompanying wrapper firmware.

The GPP source code was ported to the new system by creating a new INTEGRITY project and transferring the GPP source files from the VxWorks project. While additional effort was required to migrate to a new RTOS and TCP/IP stack, the overall effort in porting the SDR-3000 waveforms to the SDR-4000 was minimized through the use of Spectrum's *quicComm* Hardware Abstraction Library (HAL). Aside from some enhancements to the API, the *quicComm* API for the SDR-4000 platform is virtually the same as that of the SDR-3000 platform.

FPGA application code from the SDR-3000 was adapted to accommodate a modified data format and differences in the timing of certain interfaces on the SDR-4000. Other changes to the FPGA code were also implemented to take advantage of new, more powerful features of the Virtex4 FPGA devices used on the SDR-4000. For example, the digital down-converter (DDC) and up-converter (DUC) in the original digital subsystem were originally built using the hardware multipliers in Virtex-II FPGA, while the Virtex-4 family used in the new subsystem offers expanded functionality in its XtremeDSP slice.

Another issue that needed to be addressed during the migration was managing the trade-off between maximizing processing capability while minimizing power consumption. The SDR-3000 dedicates separate processors to baseband signal processing (MPC7410 PowerPC) and control functions (405GP processor). In contrast, the simpler architecture of the SDR-4000 incorporates the use of a single, low-power general-purpose processor, the MPC8541E, to minimize overall board power consumption and reduce board size.

Since less processing resources were available, optimization of signal processing algorithms, such as baseband demodulation and modulation, and merging of board control functions was required during the migration process.

The Results

While work on this project is still ongoing, it is clear that despite differences in the hardware components and operating system used in the laboratory demonstration platform (SDR-3000) and the rugged, low-power SDR demonstration platform (SDR-4000), the effort of replacing the SDR-3000 platform with SDR-4000 technology in the Tactical Military Communications Technology Demonstrator System and migrating the application code was minimized, through the use of a common hardware abstraction layer (*quicComm API*), a common communications infrastructure (*flexFabric*), and common FPGA wrappers.

The tasks associated with this technology upgrade highlighted a number of “best practices” that should be followed when planning for technology insertion in digital subsystems:

- Identify architectural differences between the original and new subsystems, especially the interfaces.
- Identify performance and capacity differences, and monitor or verify key performance parameters on the new subsystem.
- Integrate and test the application blocks on the new subsystem as independently of each other as possible.
- Schedule training to cover new hardware, firmware, and tools, in order to decrease project risk and increase work efficiency. This can include self-training activities and formal courses.
- Minimize changes to implementation and feature set application until the transition has been completed.

Conclusions

The case studies above illustrate the efficacy of the proposed architectural model in supporting technology insertion. By encapsulating the IF and baseband processing engines in a “standardized” modular architecture with well defined mechanical and electrical interfaces, supported by a well defined operating environment that is consistent from platform to platform, OEMs can accrue a significant savings in the development time and cost associated with offering new features and capabilities to their customers. This savings speeds time to market, reduces cost for the end customer, which in turn can differentiate the OEM and enhance their competitiveness.