

Reconfigurable Wideband Digital Receiver System Architecture for W-CDMA

The objective of the re-configurable wideband digital receiver system for W-CDMA described in this application note is to provide a solution for a single slot VME-based software radio system which addresses both the signal processing complexity of Wideband CDMA (W-CDMA) and the configurability to adapt to third generation (3G) standards as they emerge and evolve.

Background

The need to support broadband multimedia services over wireless infrastructure (with data rates of up to 2 Mbits/sec) is driving the development of third generation (3G) W-CDMA air-interfaces. The previous second generation (2G) digital cellular standards such as GSM, D-AMPS (IS-136) and Narrowband CDMA (IS-95) were only oriented to the delivery of speech and low bit-rate data services.

However, 3G systems will require new flexible software-defined radio architectures to support diverse data rates and quality-of-service (QoS) levels. Emerging wideband CDMA (W-CDMA) standards will offer the capability of supporting these higher data rates while maintaining downward compatibility with previous air interfaces.

Implementation of digital receiver architectures for 3G W-CDMA creates a major challenge for system architects. Researchers have analyzed the processing requirements for handling the de-spreading (rake receiver) and baseband processing for the reverse-link (mobile station handset to basestation). While there have been numerous improvements in digital signal processing (DSP) technology, these researchers have concluded that programmable DSP devices are still not sufficiently powerful enough by themselves to handle the 3000 to 6000 MIPS required to implement the full signal processing pipeline for a W-CDMA carrier. Hence designers are currently focused on a hybrid DSP plus FPGA approach. Programmable DSP chips are augmented with field programmable gate array (FPGA) devices used as co-processors to handle the high data rates required for 3G.

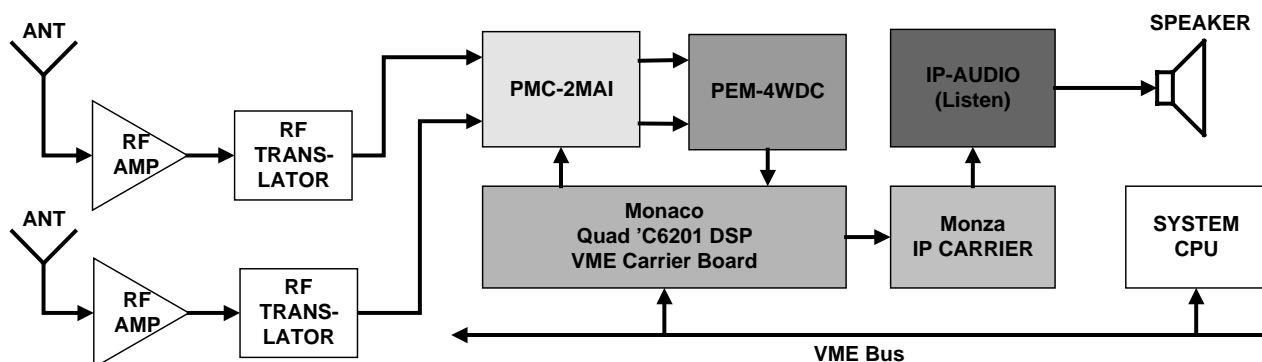
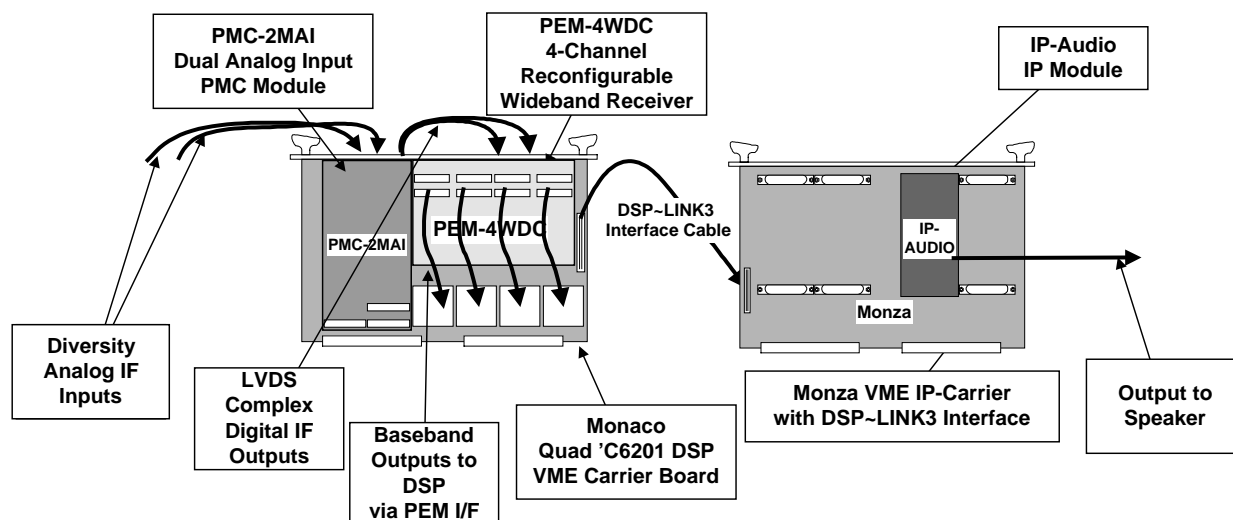
Partitioning functions between the DSP and FPGA devices is done in a fashion which optimizes the balance between cost, power dissipation, flexibility, and standards compatibility. While both FPGA and DSP devices are programmable, there are tradeoffs that make FPGAs more useful for certain functions and DSP for others. For instance, functions such as matched FIR filters and correlators, fast Fourier transforms (FFTs), Walsh and Gold long coding, Viterbi decoding, and search estimation/tracking in rake receivers are ideal for FPGA acceleration. Other bitstream processing functions like echo cancellation, de-interleaving, and phase-shift keying modulation algorithms are more appropriately assigned to the DSP.

System Requirements

- ▶ 25 MHz Input Bandwidth (using 2.5x over-sampling) for sample rates up to 65MSPS.
- ▶ Provide 2 analog IF inputs (from RF translators)
- ▶ Receiver only (reverse link)
- ▶ Need low power and noise immunity
- ▶ Provide programmable tuning and bandwidth (support 4 independently tunable complex I+Q signal outputs from the DDC section with up to 5MHz bandwidth for each carrier.
- ▶ Provide sufficient signal processing power to handle 4 separate cdma2000 or UMTS W-CDMA signal processing pipelines (one for each 5MHz carrier) including rake receiver and all baseband demodulation (including vocoder)
- ▶ Perform signal analysis and demodulation
- ▶ Provide audio output

System Solution

For this application the PEM-4WDC re-configurable wideband digital receiver can be used to create a single-slot, high-performance solution for wideband digital radio applications. See the system block configuration diagram. The key components of this system are:



Example Monaco & PEM-4WDC System Configuration for Digital Radio

Spectrum PMC-2MAI - a dual analog input module that converts analog IF signals to a stream of complex IF digital samples. Dual analog IF inputs (130kHz – 75 MHz) from a RF translator are passed to the PMC-2MAI module using front panel BNC-SMB coaxial cable connectors. The output samples from the PMC-2MAI are transferred to the PEM-4WDC using a LVDS (low-voltage differential signaling) cable assembly attached to the front panel.

Spectrum PEM-4WDC -. The PEM-4WDC is a wideband digital down converter module compatible with Spectrum's Processor Expansion Module (PEM) specification and uses both PEM sites (double width PEM) on the Monaco carrier. The PEM-4WDC accepts two digitized IF streams from Spectrum's PMC-2MAI ADC module at an input sample rate of up to 65 MHz. The IF streams are transferred from the PMC-2MAI to the PEM-4WDC on a ribbon cable using LVDS signaling for low power consumption and high noise immunity. The Graychip GC1012A downconverter is used to extract and decimate selected frequencies from the digital IF inputs. The resulting baseband data is then pre-processed by the onboard FPGA (used for de-spreading CDMA signals in this example) and fed to the FIFO buffers. Then the complex baseband output from the PEM-4WDC is forwarded over the 4 PEM (processor expansion module) interfaces to the Monaco DSP carrier for subsequent processing.

Spectrum Monaco Quad 'C6201/C6701 VME Carrier - The 4 DSP processors on this board provide tremendous power to accommodate extremely complicated baseband signal processing requirements. Each DSP processes one of the 4 output channels from PEM-4WDC which is passed directly to the DSP's external memory interface (EMIF).

Spectrum Monza VME IP Carrier – a passive VME carrier for IP (Industry Pack modules). This carrier is interfaced to the Monaco board using the DSP-Link3 interface cable. The Monza carrier is used to host the Spectrum IP-Audio module (described below) to provide selective audio monitoring of a de-modulated/decoded audio channel. This audio data is passed over the DSP-Link3 interface directly to the IP-Audio module (bypassing the VME system bus).

Spectrum IP-Audio – an IP (Industry Pack) module which is used in this configuration to provide a digital-to-analog DAC output for monitoring a de-modulated/decoded audio channel.

Refer to the block diagram from found in the PEM-4WDC datasheet from this handbook.

Each of the 4 Virtex XCV400 FPGA devices used on the PEM-4WDC features a flexible, regular architecture (comprised of an array of configurable logic blocks surrounded by programmable input/output blocks, all interconnected by a rich hierarchy of fast, versatile routing resources). The Virtex XVC400 FPGA has 468,252 system gates. The Virtex XVC400 FPGA is SRAM-based, and is customized by loading configuration data into internal memory cells. FPGA core libraries to support Wideband CDMA will be available soon from third parties such as Agilent, Elanix and Synopsis.

The **Monaco/PEM-4WDC/PMC-2MAI** combination results in the highest I/O channel and processing density in a single slot wideband digital radio solution. Furthermore, Spectrum digital radio I/O products are optimized to maximize the data flow between the digital radio receiver and the DSP processing resources.