

DSP Technology Optimizes Multi-Channel Digital Receivers

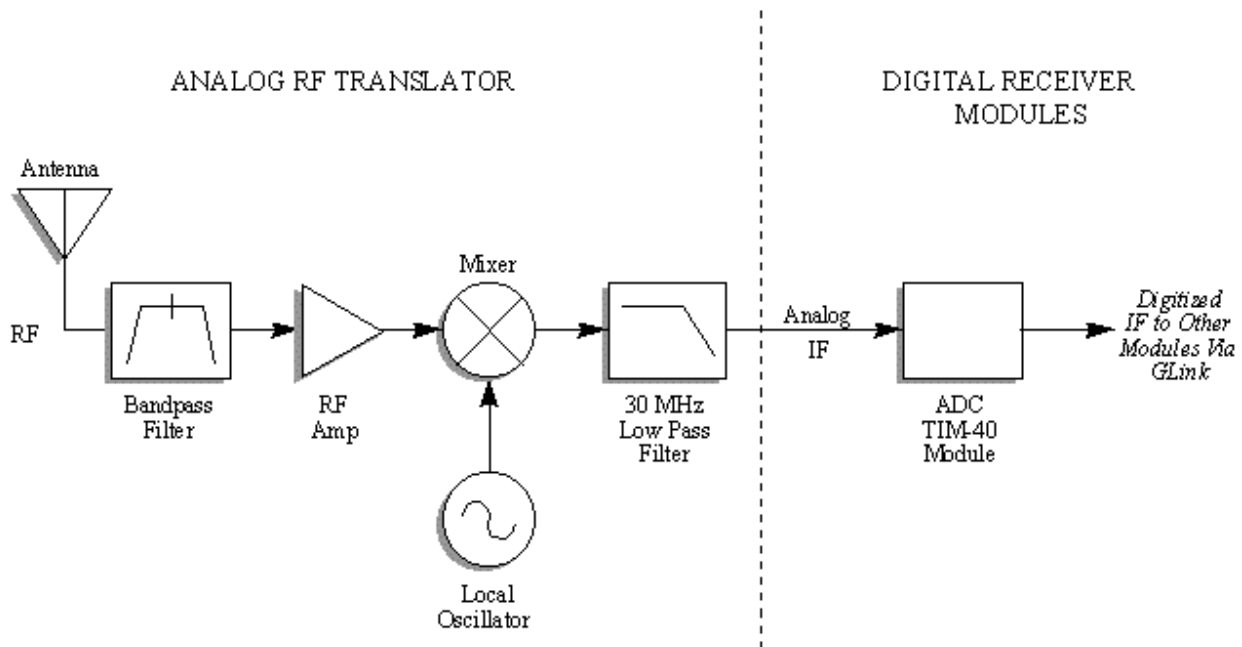
By Toby Haynes, Senior Technical Lead
Spectrum Signal Processing

Digital signal processing (DSP) is rapidly transforming the architecture of wireless communications systems. While digital technology can provide an elegant design solution, it is highly dependent on unobstructed data communications between the DSPs, host CPU and other portions of the system. Ensuring high data throughput is challenging but is being simplified by modular digital receiver architectures.

Digital receiver advantages

In their basic forms, analog and digital receivers are nearly identical in that they capture the incoming RF signals the same way. However, rather than an analog demodulator, the digital receiver uses an ADC and DSP to downconvert and process the signal.

Figure 1. Block diagram showing where analog components end and digital ones begin



Digital filtering replaces analog hardware filtering traditionally accomplished by Surface Acoustics Wave (SAW), ceramic, or crystal filters. Filtering options are virtually limitless and performance of even basic digital filters can be as good as the best analog filters, and fewer components are required to achieve it as well.

Digital drop receivers

In order to provide high levels of functional integration and simplify digital receiver design, manufacturers have produced chip sets that together form a subsystem called a Digital Drop Receiver (DDR) or digital tuner.

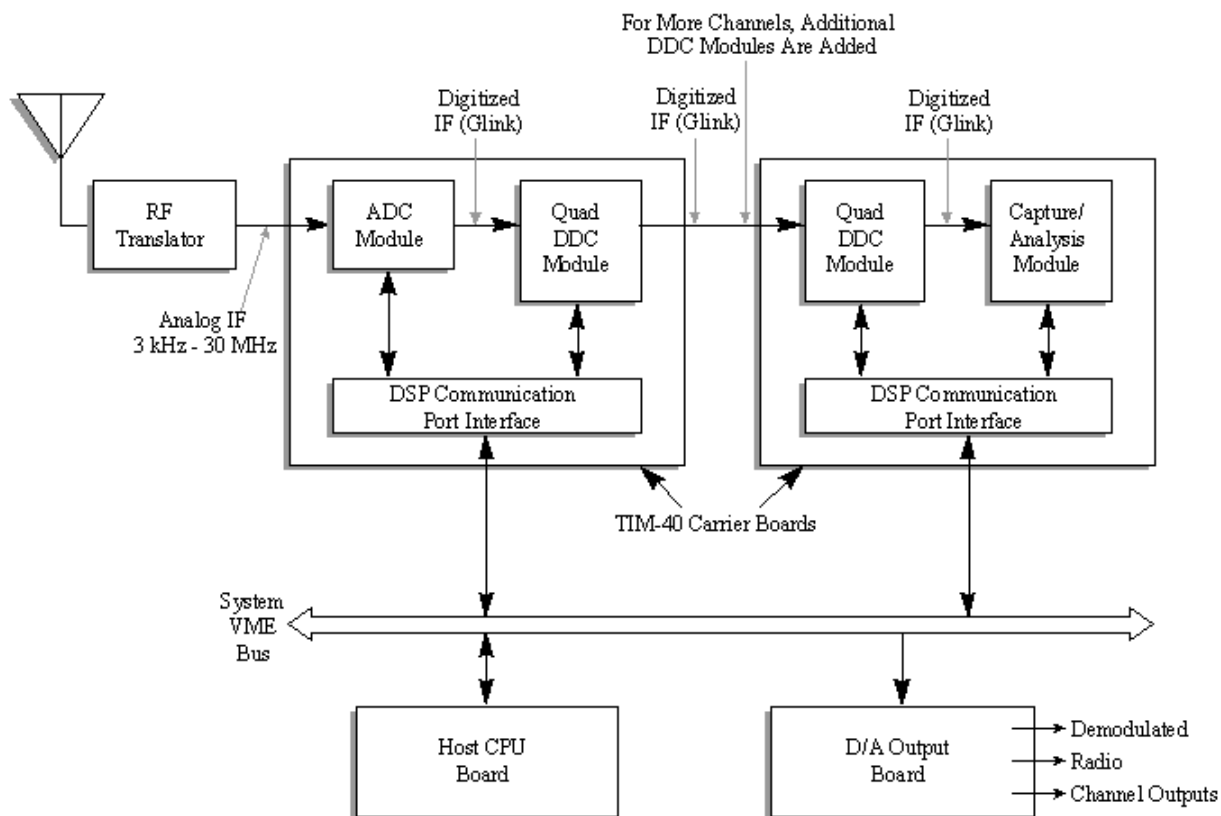
The DDR is a dedicated signal processing system that rejects unwanted signals, selecting the signals of interest and reducing their data rate (called decimation) to baseband so that they may be effectively processed by DSPs. In addition, the DDR employs sophisticated digital filtering that avoids the use of complex analog filter components. The ability to provide filtering digitally makes it much easier to provide a certain set of filter characteristics that do not change over time.

Like all digital designs, filters require no adjustment or tweaking to achieve the desired level of performance. This provides significant benefits in component cost, design, manufacturing, and test time, which increases production throughput.

Digital Down Conversion

In current digital receiver designs, the ADC digitizes the IF signal and passes it to DSPs for channel filtering and demodulation. In such a system, the IF bandwidth is limited by the available DSP processing power. Undersampling of the IF is commonly used to keep the sample rate low enough so that DSPs can keep up.

Figure 2. A Receiver Using Digital Down Conversion



By employing digital down conversion ahead of the DSPs, a single processor needs to handle only a fraction of the total IF bandwidth. With this approach, a narrow bandwidth from the digitized 30 MHz wide IF is extracted by the digital down converter, which then delivers to the DSP a baseband version at greatly reduced sample rates. The DSP software implements filtering and demodulation of the small number of radio channels within the down-converted bandwidth. By utilizing multiple digital down converters and DSPs, numerous channels can be received simultaneously from a single digitized IF.

In addition to its obvious benefits, digital down conversion provides exceptional frequency control—down to a fraction of a Hertz--and accomplishes frequency changes within a few sample clock cycles. Digital down conversion also has excellent noise performance and allows any bandwidth to be selected through digital filtering without negatively impacting group delay. The In-phase (I) and Quadrature (Q) relationship of the complex baseband data stream can be maintained to exactly 90 deg. through these digital techniques.

Digital Receiver Architectures: An Example

There are many ways to configure digital receivers. However, they almost invariably rely on a building-block approach, the configuration of which depends on the digital signal processing devices chosen. A typical multichannel, narrowband receiver architecture utilized by Spectrum Signal Processing Inc. reflects this approach. It consists of three TIM-40 modules that can be combined in various ways to produce a bus-independent digital drop receiver (DDR).

Analog Input Module

The first module in the set digitizes a 3 kHz-to-30 MHz IF signal delivered via a 50-ohm coaxial cable. By digitizing signals closer to the antenna (either the entire 30 MHz HF band, or a 30MHz IF portion of the band of interest), a traditionally fixed function analog stage of the radio receiver, is brought under software control. Such programmable soft radio designs require not only fewer MIPS of processing power than previous technology approaches, but also provide flexible spectral, modulation and audio information in support of changing end-user needs.



An analog input TIM-40 module (TIM-MAI)

The IF signal comes from an RF translator that uses conventional analog circuits (local oscillator, mixer and filters) to convert UHF or microwave RF signals from the antenna down to frequencies below 30 MHz. The IF signal is then filtered, and gain control is applied. A clipping monitor detects when the input voltage exceeds a threshold of 72% of full scale (2Vpp), and adds the number of threshold crossings to the 16-Bit counter. The counter is reset and read with a C4x communication port from another module (TIM-40 communications port 1). The C4x then determines the amount of attenuation necessary on the input signal and adjusts the Gain Controller in 2 dB steps within a 30 dB range. The ADC then samples the conditioned IF signal at up to 70 Megasamples per second with 10-bit resolution. The IF signal, now digital, is communicated to other modules over a high-speed (1.4 Gb/s) serial bus called GLink.

GLink Serial Bus

The A/D data is distributed from the first module to the next using Glink and so forth to create a network of DDCs. The GLink transmitter is capable of transmitting data up to 6 feet on a 50 ohm coaxial cable. A programmable “DDC sync” signal is transmitted on GLink to reset each digital down converter module on the GLink network for coherent DDC processing.

Digital Down Converter Modules

The next module in the system accepts the digitized wideband IF from the ADC module and simultaneously tunes, downconverts and processes four narrowband channels. The down conversion module consists of a double-width TIM-40 module with four Harris HSP50016 digital down converter chips and two Texas Instruments TMS320C44 DSPs. Two DDCs are controlled by one C44 Global bus and the other two are controlled by the other C44 global bus. There are also two GLink transmitters and two GLink receivers on the module, which allow the down converter to receive and retransmit the digitized IF to other down converter modules in the system.



A quad digital down converter TIM-40 module (TIM-DDC).

The HSP50016 accepts samples at up to 70 megasamples/second with 16-bit resolution. Input samples are multiplied by a complex sinusoid at a frequency that is programmable from DC to half the input sample frequency. The output is a lowpass-filtered, decimated signal with identical real filters for the I and Q signal components.

Lowpass filtering is performed by a programmable, high-decimation digital filter followed by an FIR filter with a fixed decimation rate. Bandwidth selectivity ranges from 507 kHz to 294 Hz based on an input sample rate of 70 megasamples/second. The output of the downconverter is either a real data stream or a complex quadrature data stream in serial format that can be digitally demodulated or processed.

Each of the HSP50016 down converters can be tuned to a narrowband signal within the IF bandwidth. The low-sample-rate quadrature baseband signals from the device are sent to the communication ports of the TMS320C44. The DSPs have 512 Kbytes of SRAM, and can execute demodulation or signal analysis algorithms in real-time.

The last module in the system provides fast capture and analysis of the entire digitized IF spectrum. It utilizes a hardware-controlled, double-buffering scheme that allows the module's GLink receiver to stream the incoming digitized IF to one DRAM bank while the TMS320C44 processes another bank that was previously loaded. The DSP can search for radio signals or perform other functions on the IF signal and communicate the results to the host computer or other TIM-40 modules hosting C40 or C44 DSPs with SRAM, DRAM or EDRAM through communications ports.

An unlimited number of down converter modules can be utilized to sample the digital IF on the GLink bus, each one simultaneously downconverting and processing up to four channels. Since the down converter module can retransmit IF signals in daisy-chain fashion, an unlimited number of narrowband channels can be

received. The capture and analysis module can also terminate GLink and receive and process the entire IF spectrum if desired. As a result, the three modules together can be configured to form a scaleable signal processing system that is flexible enough to accommodate a wide variety of system designs. The DDR suite is applicable to VMEbus, PCI and VXI-based systems since it is implemented on standard TIM-40 mezzanine modules, which may be installed on TIM-40 capable carrier boards for any bus architecture.

Future Trends

It is exciting to imagine an almost completely digital radio that accepts signals directly from the antenna without intervening analog components. Unfortunately, this scenario is not currently possible for several reasons, the most limiting of which is the dynamic range that an ADC would require to deal with the immense number of signals it would be presented.

In addition, it would have to perform its processing at the receive frequency, perhaps 2 GHz or even higher, a feat impossible today. Even if it were possible, unacceptable compromises in receive sensitivity, selectivity, and image rejection would still be required. For this reason, the digital components are moved down the signal chain to the IF stages. With far fewer unwanted signals to reject, the ADC is much less likely to become saturated, needs less dynamic range, and still reduces complexity by eliminating analog components in IF stages.

Conclusion

The DDR approach taken by Spectrum has two main advantages:

- 1) The Coaxial-based digital “Broadcast” of the digitized RF spectrum can be made available to many DSP/DDC systems simultaneously to allow for handling of multiple channels in real time, thus creating a “one-tuner-with-many-signals” system.
- 2) The DSPs are equipped with multiple independent communications ports which allow for inter-processor communications as well as data presentation to the host concurrent with signal processing activities.

Digital signal processing will undoubtedly play an increasing role in the design of receiver systems for wireless communications. As the number of channels and data rates in wireless services increase, so too will the demand for high-speed DSP architectures to implement them. This demand is likely to be met by highly-integrated, modular components that are designed to function optimally together to maintain true real-time signal processing performance.

Multiprocessing

One of the keys to achieving real-time signal processing performance in digital receivers is to harness the power of DSPs in the most effective manner by achieving optimum processor-to-processor communication throughput.

The architectures of some floating-point DSPs are optimized for parallel processing, which facilitates the real-time performance that wireless communication systems require. DSPs designed for scaleable parallel processing have multiple high-speed data and memory buses, a number of I/O interfaces and on-chip controllers for inter-processor communication, and have instruction sets that execute instructions very fast. One of the most widely-used DSPs for this application is the TMS320C40 from Texas Instruments. Each of its communication ports operate at up to 20 Mbyte/s, which facilitates uninterrupted inter-processor communication even when multiple DSPs are used.

Texas Instruments created a system-level specification for multiprocessing modules called TIM-40, which has become the industry standard module architecture for this device. The module contains one or more TMS320C40 DSPs, I/O interfaces, and memory, and brings the device's communication ports out to a connector to interface with other modules. The host-to-DSP bus is usually VMEbus, ISA, or PCI. TIM-40 modules can be configured in virtually any number to produce the real-time performance required by digital receivers.

About the author



Toby K. Haynes, Senior Technical Lead

B.A.Sc in Electrical Engineering from the University of British Columbia, 1985. Currently designing DSP and digital radio hardware for the Military, Aerospace and Commercial (MAC) Group of Spectrum Signal Processing, Inc. Previously Haynes designed DSP and VME bus hardware for Motorola's Wireless Data Group. He can be reached at 301-918-2522.