



Indy

**F3 Processor Board
Technical Reference**

Document Number 500-00350

Revision 1.01

August 1998

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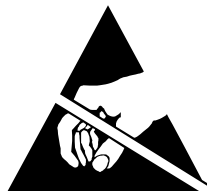
- A concise description of the problem
- The name of all Spectrum hardware components
- The name and version number of all Spectrum software components
- The minimum amount of code that demonstrates the problem
- The version number of all software packages, including compilers and operating systems

Preface

Spectrum Signal Processing offers a complete line of DSP hardware, software and I/O products for the DSP Systems market based on the latest DSP microprocessors, bus interface standards, I/O standards and software development environments. By delivering quality products, and DSP expertise tailored to specific application requirements, Spectrum can consistently exceed the expectations of our customers. We pride ourselves in providing unrivaled pre and post sales support from our team of application engineers. Spectrum has excellent relationships with third party vendors which allows us to provide our customers with a more diverse and top quality product offering.



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As Spectrum's hardware products are static sensitive, please take precautions when handling and make sure they are protected against static discharge.

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1 Introduction

1.1. Purpose of This Manual

This manual describes the features, architecture, and specifications of the *Indy F3 Processor Board*. It will help you understand how the function libraries described in the *F3 Processor Board User Guide* communicate with the board. You can also use this information to program the board at a driver level, extend the standard hardware functionality, or obtain more information to do custom configurations.

1.2. Reference Documents

This guide is meant to be used with the following documents:

- *Indy F3 Processor Board User Guide* available from Spectrum
- *TMS320C3x Users Guide* available from Texas Instruments
- DSP~LINK3 specification available from Spectrum
- Technical documentation for any installed DSP~LINK3 analog module or DSP~LINK3 peripheral board.

2 Hardware Overview

The F3 Processor Board is a half-length ISA expansion board equipped with a single TMS320C32 DSP. DSP~LINK3 allows the F3 Processor Board to host compatible DSP~LINK3 expansion modules, to add such features as analog I/O.

The F3 Processor Board is available in a stand-alone or in an ISA bus version. (It is not possible to change one version to another.)

Stand-Alone Configuration In the stand-alone configuration, a Flash ROM is included for booting user application code. An external power connector is included to provide power to the board.

ISA Bus Configuration In the ISA bus configuration, the board is meant to be installed in a PC computer via its 16-bit ISA bus card edge connector. Dual Port RAM (DPRAM) is included with this configuration as the memory mapped interface between the F3 Processor Board and the ISA bus. Because there is no Flash ROM, this configuration does not operate in a stand-alone mode.

2.1. Features

The following features are common to all F3 Processor Board configurations:

- Memory Bank 0: 32-bit SRAM (0K, 128K, or 512K)
- Memory Bank 1: 32-bit SRAM (32K or 128K)
- JTAG interface header (also known as Modular Port Scan Device, MPSD)
- Buffered serial port interface
- TTL digital I/O interface
- TCLK_x signal support
- DSP~LINK3 ribbon cable connector
- DSP~LINK3 module connector

Features unique to each F3 Processor Board configuration are given in the following list:

Stand-Alone Configuration	ISA Bus Configuration
<ul style="list-style-type: none"> • 8-bit Flash ROM (128K or 512K) • Power up reset circuit • External power connector (J10) 	<ul style="list-style-type: none"> • 2K of 16-bit Dual Port RAM (DPRAM)

2.2. Board Layout

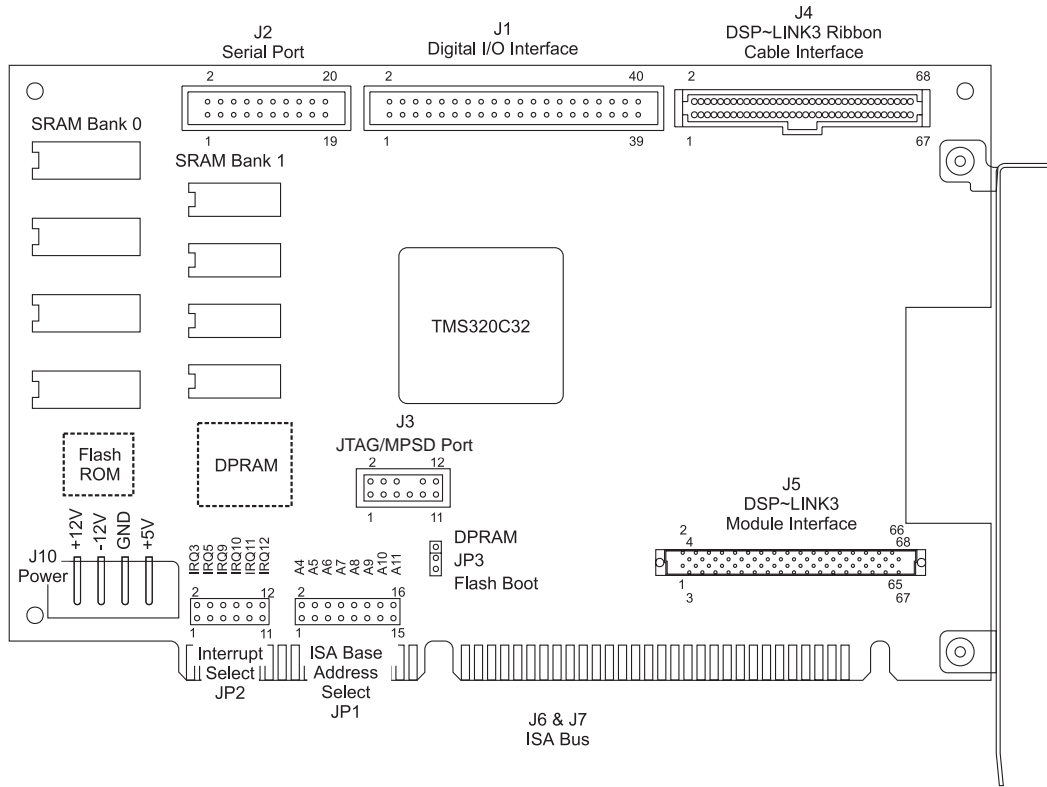


Figure 1 F3 Board Layout

Table 1 F3 Jumper Block Summary

Jumper Block	Description
JP1	ISA bus base address
JP2	ISA bus interrupt select (IRQx)
JP3	DSP boot source

Default jumper settings for the different F3 Processor Board configurations are shown in the following figure.

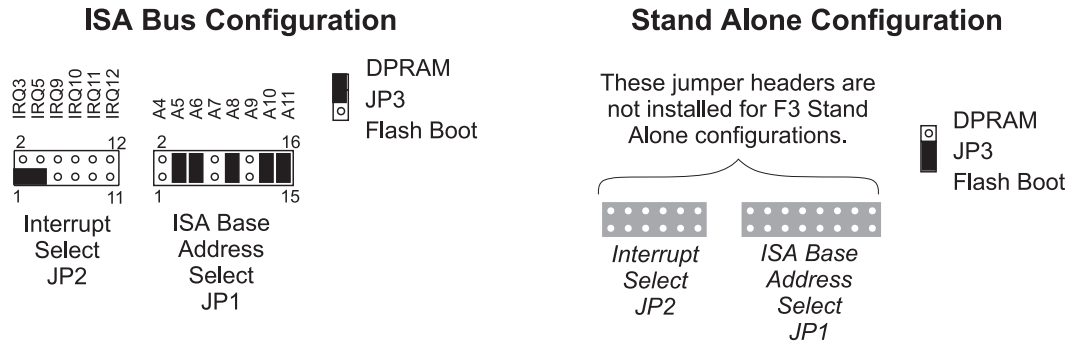


Figure 2 Default Jumper Settings

Table 2 F3 Connector Summary

Connector	Interface	Description
J1	Digital I/O	DSP memory mapped configurable digital I/O line interface
J2	Serial Port	Buffered serial port interface from the DSP
J3	JTAG Port	JTAG Emulation port direct from the DSP (also known as Modular Port Scan Device, MPSD)
J4	DSP~LINK3	DSP memory mapped DSP~LINK3 ribbon cable interface
J5	DSP~LINK3	DSP memory mapped DSP~LINK3 Module interface
J6 & J7	ISA Bus	ISA bus card edge connector for ISA bus configuration only
J10	Power	External power connector for stand-alone configuration only

2.3. Architecture

The following figure shows a block diagram of the F3 Processor Board.

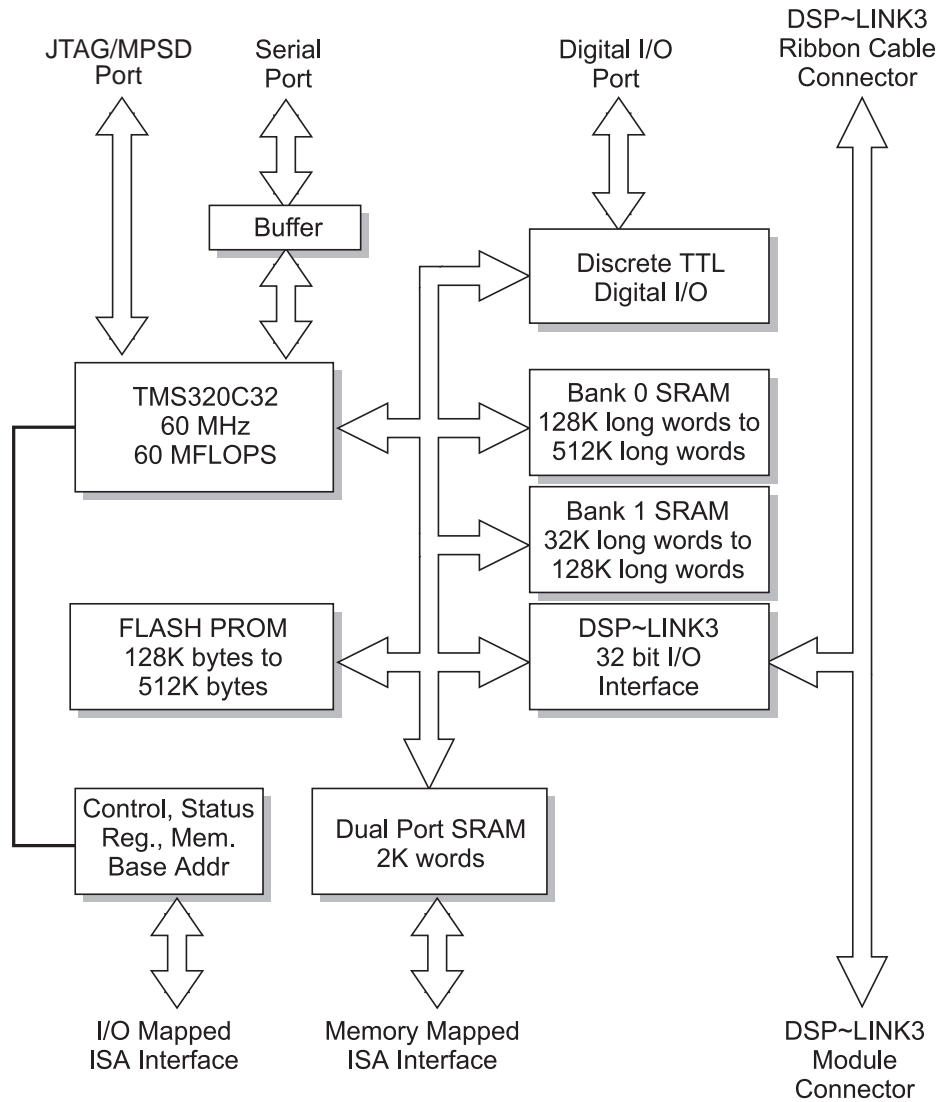


Figure 3 F3 Block Diagram

3 Installation

3.1. For ISA Bus Operation

When configured for ISA bus operation the F3 Processor Board occupies an ISA AT expansion slot of a PC computer.

3.1.1. Requirements

- PC computer with an available ISA bus AT expansion slot running Microsoft® Windows95 or Windows NT
- F3 Processor Board host driver, host application library, and example software
- Texas Instruments' Floating point development tool software (compiler and debugger)

3.1.2. Configuration

When using the F3 Processor Board as an ISA bus device configure the on board jumpers according to the following table

Table 3 ISA Bus Configuration Jumper Settings

Jumper	Description	Configuration
JP1	ISA bus base address	Set address bits A11 to A4 on the jumper block to a free location in the ISA I/O address range. Default = 0x290. Jumper installed = 0; un-installed = 1
JP2	ISA bus interrupt select	Set a single jumper to the IRQ line that the board will use to interrupt the host PC over the ISA bus. Default = none.
JP3	DSP boot source	Install the jumper across pins 1 and 2 (DPRAM).

3.1.3. Connection

After the jumpers on the F3 Processor Board have been configured, it can be installed in a PC and any other connections can be made.

1. Attach the serial port, digital I/O, JTAG, DSP~LINK3 module, and/or DSP~LINK3 cables to the board if you are using them.
2. Install the F3 Processor Board into an empty AT slot of the PC computer. **Ensure that the PC is powered OFF!**

3.2. For Stand-Alone Operation

When configured for stand-alone operation the F3 Processor Board only requires a power cable to be connected to the J10 power connector to operate. The board is reset when power is supplied.

3.2.1. Requirements

- Regulated power supply able to supply +5 VDC, +12 VDC, -12 VDC, and ground to the PC hard disk type power connector J10. Refer to figure 1 for the proper power connections.
- Application code within the Flash ROM

3.2.2. Configuration

When using the F3 Processor Board as a stand-alone device configure the on board jumpers according to the following table

Table 4 Stand-Alone Configuration Jumper Settings

Jumper	Description	Configuration
JP1	ISA bus base address	Jumper block not installed in stand-alone configuration
JP2	ISA bus interrupt select	Jumper block not installed stand-alone configuration
JP3	DSP boot source	Install the jumper across pins 2 and 3 for the board to boot from Flash ROM.

3.2.3. Connection

After the jumpers on the F3 Processor Board have been configured, the board can be installed into a system and any other required connections can be made.

Caution: Ensure that nothing comes in contact with the ISA bus card edge connector on the F3 Processor Board or the board can be damaged.

1. Attach the serial port, digital I/O, JTAG, and/or DSP~LINK3 cables to the F3 Processor Board if you are using them.
2. Attach the power cable to connector J10.

3.3. Adding a DSP~LINK3 Module

DSP~LINK3 modules can be added to the DSP~LINK3 module site as shown in the following figure.

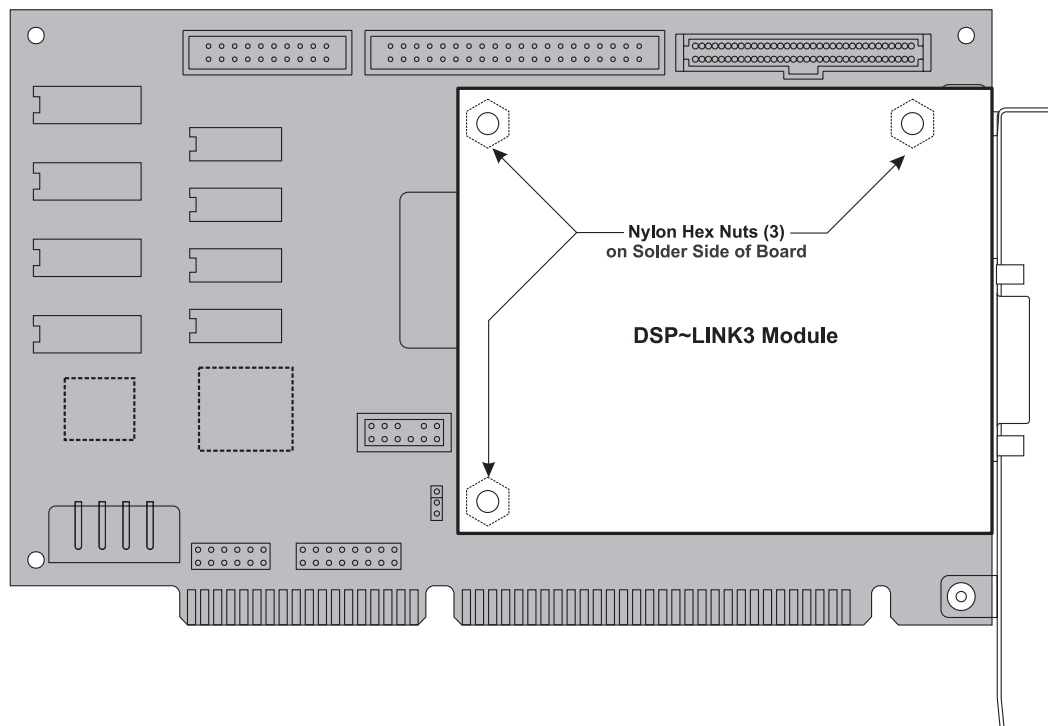


Figure 4 Module Installation

Note: Before handling the F3 Processor Board or a module, ensure that you and the components are properly grounded to prevent damage from electrostatic discharge.

1. If the module that you are installing has its own end plate bracket, remove the end plate bracket that is attached to the F3 Processor Board.
2. Position the module on to the F3 Processor Board using the nylon mounting posts.
3. Secure the module to the F3 Processor Board by screwing the three 3mm nylon hex nuts to the mounting posts.
4. Screw the end plate of the module to the F3 Processor Board.

4 TMS320C32 DSP

The board supports Texas Instruments TMS320C32 Digital Signal Processor. The board has been designed operate with following configuration:

- 60 MHz maximum clock rate
- Fixed 32-bit data accesses in STRB0's address space
- 16- or 32- bit data accesses in STRB1's address space
- Fixed 32-bit program word fetches
- Microcomputer boot loader mode

Note: Although the TMS320C32 can support different data sizes in the same physical memory, this is not supported on the F3 Processor Board.

4.1. Reset

The active-low board RESET is generated by:

- A write to ISA Control Register setting the reset bit
- Initial power-on of the ISA configured board
- The power-on reset circuit installed on the stand-alone version of the F3 Processor Board.

4.2. Interrupts

TMS320C32	
Interrupt Line	Description
/INT0	Logical OR'ed result of the DSP~LINK3 interface's /INT0 and /INT1 lines
/INT1	Controlled by the ISA interface's Interrupt Register. An ISA write to the Interrupt Register asserts /INT1 for one DSP H1 cycle
/INT2	Connected to the interrupt pin from the Digital I/O interface
/INT3	Logical OR'ed result of the DSP~LINK3 interface's /INT2 and /INT3 lines

4.3. DSP Booting

The boot source for the DSP depend on how the F3 Processor Board is configured. In stand-alone configuration, the DSP boots from the Flash ROM; in ISA-bus configuration the DSP boots from DPRAM.

The memory location that the TMS320C32 boots from is determined from the state of its /INT0 and /INT3 lines at the release of reset. Jumper J3 sets the state of these pins so that the DSP boots from one of two memory locations in the F3 Processor Board's memory map. One location contains the Flash ROM and the other contains the DPRAM memory space. See the memory map section.

Jumper J3 sets the boot source as follows:

- DPRAM is selected as the boot source by placing a jumper across pins 1 and 2 of JP3. /INT2 is held low during and after reset until the first access to the DPRAM.
- Flash ROM is selected as the boot source by placing a jumper across pins 2 and 3 of JP3; /INT0 is held low during and after reset until the first access to the Flash ROM.

Note: Flash ROM is only installed on the stand-alone configuration of the F3 Processor Board.

4.4. XF0 Flag

The DSP's general purpose I/O pin XF0 is used to reset any devices connected to the DSP~LINK3 interface. The pin is configured via the DSP's IOF register. By default it is configured as an input after reset. The pin is connected to the DSP~LINK3 interface reset signal via a buffer component and must be set to operate as an output. By default, after a board reset the DSP~LINK3's /RESET line is held low (asserted).

4.5. Timers

The TCLK0 and TCLK1 timer pins are connected via a buffer to the Digital I/O Interface connector.

TCLK0 is wired as an input. Therefore the DSP application software should only set this pin to operate as an input. By default, this pin is an input after reset.

TCLK1 is wired as an output. Therefore the DSP application software should only set this pin to operate as an output. By default, this pin is an input after reset.

4.6. Serial Port

The Serial Port is connected, via a buffer, to a 2x10 pin shrouded connector.

4.7. JTAG Port

The JTAG emulation pins are connected to a 2 x 6 pin connector and pulled up by 20k resistors as prescribed in the *TMS320C3x User's Guide*.

5 Memory

The memory resources of the board consist of:

- One or two banks of SRAM
- DPRAM for ISA bus configurations
- Flash ROM for stand alone configurations

The required wait-states are inserted by on-board logic and are transparent to the user.

5.1. SRAM

The two banks of SRAM operate with zero wait state accesses. Check the installed memory and then refer to the memory maps to determine valid SRAM address spaces.

Bank 0 0/128/512K x 32 zero-wait-state SRAM made up of 4 - 128K/512K x 8, 15ns, revolutionary pin out, SRAM components.

Bank 1 32/128K x 32 zero-wait-state SRAM made up of 4 - 32K/128K x 8, 15ns, evolutionary pin out, SRAM components.

5.2. DPRAM

The 2K x 16 DPRAM is made up of a single 35 ns component. It is the interface between the ISA bus and the DSP. DPRAM access from the DSP requires two-wait-states.

The DPRAM is mapped to the DSP's /STRB1 location on a 16-bit data bus. Therefore the DSP's STRB1 Control Register must be configured to access the DPRAM with a physical memory width of 16 bits and as a 16- or 32-bit data type.

5.3. Flash ROM

The Flash ROM memory is made up of a single 120ns 128K x 8 (AM29F010) or 512K x 8 (AM29F040) device. Flash ROM access from the DSP requires four wait-states. It is only installed on the stand-alone configuration of the F3 Processor Board.

When programming the Flash ROM with the utility provided in the F3 Processor Board development kit, pay particular attention to the sequences required to program the component successfully and ensure that your boot code begins at address 0000 1000h.

5.4. DSP Memory Maps

The memory map of the F3 Processor Board varies, depending upon the amount of Flash ROM and memory in SRAM banks 0 and 1. The following tables show the possible memory maps for different board configurations.

Figure 5 Memory Map with SRAM Bank 0 = 0K

No STRB	Reserved by DSP, 1000 Words, Boot Loader	0x000000 0x000FFF
/STRB0	Flash ROM Boot Code: (8 bit data width) (Stand-alone version only) 128K Words, or	0x001000 0x020FFF
	Reserved	0x100000 0x11FFFF
	Digital I/O Interface (32 bit data width), Input/Output	0x200000
	Digital I/O Interface (32 bit data width), Input Only	0x220000
	DSP-LINK 3 (32 bit data width), Standard Operation	0x300000 0x30FFFF
	DSP-LINK 3 (32 bit data width), Standard Fast Operation	0x400000 0x40FFFF
	DSP-LINK 3 (32 bit data width), /ASTRB cycle	0x500000 0x50FFFF
	DSP-LINK 3 (32 bit data width), RDY Controlled Operation	0x600000 0x60FFFF
	DSP to ISA Interrupt Register	0x700000
	None	Reserved by DSP, 6K Words, Peripheral Bus Memory-Mapped Registers
Reserved by DSP, 26K Words		0x809800 0x80FFFF
Reserved by DSP, 327K Words		0x830000 0x87FDFF
DSP Internal RAM Block 0, 256 Words		0x87FE00 0x87FEFF
DSP Internal RAM Block 1, 256 Words		0x87FF00 0x87FFFF
/STRB0		Bank 1 SRAM: (32 bit data width), 32K Words, or
	128K Words	0x89FFFF
	/STRB1	Dual Port RAM boot: (16 bit data width), 2K Words (ISA-bus version only)

Figure 6 Memory Map with SRAM Bank 0 = 128K

No STRB	Reserved by DSP, 1000 Words, Boot Loader	0x000000
		0x000FFF
/STRB0	Flash ROM Boot Code: (8 bit data width) (Stand-alone version only) 128K Words, or ----- 512K Words	0x001000
		0x020FFF
	0x080FFF	
	Reserved	0x100000
		0x107FFF
	Digital I/O Interface (32 bit data width), Input/Output	0x200000
	Digital I/O Interface (32 bit data width), Input Only	0x220000
	DSP-LINK 3 (32 bit data width), Standard Operation	0x300000
	0x30FFFF	
	DSP-LINK 3 (32 bit data width), Standard Fast Operation	0x400000
	0x40FFFF	
DSP-LINK 3 (32 bit data width), /ASTRB cycle	0x500000	
0x50FFFF		
DSP-LINK 3 (32 bit data width), RDY Controlled Operation	0x600000	
0x60FFFF		
DSP to ISA Interrupt Register	0x700000	
No STRB	Reserved by DSP, 6K Words, Peripheral Bus Memory-Mapped Registers	0x808000
		0x8097FF
	Reserved by DSP, 26K Words	0x809800
		0x80FFFF
	Reserved by DSP, 327K Words	0x830000
		0x87FDFF
DSP Internal RAM Block 0, 256 Words	0x87FE00	
0x87FEFF		
DSP Internal RAM Block 1, 256 Words	0x87FF00	
0x87FFFF		
/STRB0	Bank 0 SRAM: (32 bit data width), 128K Words	0x880000
		0x89FFFF
	Bank 1 SRAM: (32 bit data width), 32K Words, or ----- 128K Words	0x8A0000
0x8A7FFF,		
0x8BFFFF		
/STRB1	Dual Port RAM boot: (16 bit data width), 2K Words (ISA-bus version only)	0x900000
		0x9007FF

Figure 7 Memory Map with SRAM Bank 0 = 512K

No STRB	Reserved by DSP, 1000 Words, Boot Loader	0x000000 0x000FFF	
/STRB0	Flash ROM Boot Code: (8 bit data width) (Stand-alone version only) 128K Words, or ----- 512K Words	0x001000 0x020FFF 0x080FFF	
	Bank 1 SRAM: (32 bit data width), 32K Words, or ----- 128K Words	0x100000 0x107FFF 0x11FFFF	
	Digital I/O Interface (32 bit data width), Input/Output	0x200000	
	Digital I/O Interface (32 bit data width), Input Only	0x220000	
	DSP~LINK 3 (32 bit data width), Standard Operation	0x300000 0x30FFFF	
	DSP~LINK 3 (32 bit data width), Standard Fast Operation	0x400000 0x40FFFF	
	DSP~LINK 3 (32 bit data width), /ASTRB cycle	0x500000 0x50FFFF	
	DSP~LINK 3 (32 bit data width), RDY Controlled Operation	0x600000 0x60FFFF	
	DSP to ISA Interrupt Register	0x700000	
	No STRB	Reserved by DSP, 6K Words, Peripheral Bus Memory-Mapped Registers	0x808000 0x8097FF
		Reserved by DSP, 26K Words	0x809800 0x80FFFF
Reserved by DSP, 327K Words		0x830000 0x87FDFF	
DSP Internal RAM Block 0, 256 Words		0x87FE00 0x87FEFF	
DSP Internal RAM Block 1, 256 Words		0x87FF00 0x87FFFF	
Bank 0 SRAM: (32 bit data width), 512K Words		0x880000 0x8FFFFFFF	
/STRB1	Dual Port RAM boot: (16 bit data width), 2K Words (ISA-bus version only)	0x900000 0x9007FF	

6 Interfaces

The F3 supports the following interfaces:

- ISA
- JTAG Port
- Serial Port
- Digital I/O
- DSP~LINK3.

6.1. ISA Interface

The ISA interface is designed to operate with a nominal ISA bus speed of 8.33 MHz and consists of:

- I/O mapped control and status register
- I/O mapped interrupt register
- Memory mapped Dual Port RAM (DPRAM)

6.1.1. ISA Interface Register Map

Address	Function
Base Address + 0	Control Register (Write Only) Status Register (Read Only)
Base Address + 2	DPRAM Base Address Register. Write to this register to set up the most significant 16 bits of the memory map. Example: writing 0D00h sets the base address to 0D00 00h
Base Address + 4	Interrupt Register. A Write causes a pulse on the DSP's /INT1 pin, a Read clears any latched interrupt from the DSP to the PC.

Control Register

I/O base address + 0, Write only

D7	D6	D5	D4	D3	D2	D1	D0
				8/16#		DPRAM_EN#	RESET#

RESET# Bit D0 resets the board's DSP and logic. Active Low.

- 0 holds the DSP in reset (default)
- 1 releases the DSP from reset

DPRAM_EN# Bit D1 enables the memory mapped DPRAM port on the ISA bus. Active Low.

- 0 enables the DPRAM port on the ISA bus
- 1 disables the DPRAM port on the ISA bus (default)

8/16# Bit D3 selects the ISA bus memory mapped interface width. It is best to use 16-bit.

- 0 sets the ISA bus interface for 16-bit operation (default)
- 1 sets the ISA bus interface for 8-bit operation

The ISA configuration register is set to its default settings after the board is powered on or after an ISA reset cycle.

Status Register

I/O base address + 0, Read only

D7	D6	D5	D4	D3	D2	D1	D0
DPBOOT#	FLASHBOOT#	INTPC	BOOT_DONE	8/16#		DPRAM_EN#	RESET#

- RESET#** Bit D0 indicates the DSP reset line status.
- 0 = DSP in reset
 - 1 = DSP released from reset
- DPRAM_EN#** Bit D1 indicates the DPRAM enable status.
- 0 = DPRAM port on the ISA bus enabled
 - 1 = DPRAM port on the ISA bus disabled
- 8/16#** Bit D3 indicates the ISA bus memory interface width.
- 1 = 8 bits wide
 - 0 = 16 bits wide
- BOOT_DONE** Bit D4 indicates whether the DSP has started a boot cycle.
- 1 = DSP has started a boot cycle
 - 0 = DSP has not started a boot cycle
- INTPC** Bit D5 indicates the interrupt line Status from the DSP to the PC.
- 1 = Interrupt asserted
 - 0 = No interrupt
- FLASHBOOT#** Bit D6 indicates if DSP boot source is Flash ROM.
- 0 = Boot from Flash ROM
 - 1 = Not booted from Flash ROM
- DPBOOT#** Bit D7 indicates if DSP boot source is the ISA bus through DPRAM.
- 0 = Boot from DPRAM
 - 1 = Not booted from DPRAM

DPRAM Memory Space Base Address Register

I/O base address + 2, Write-only

The value set in this register determines where in the ISA memory address space the board's DPRAM is mapped. The address must be within ISA memory address range of 0A0000 to 0DFFFF. On a 4K boundaries; example: 0D0000, 0D1000, 0D2000, 0D3000, etc..

Therefore to map the board's DPRAM base address to 0D1000 of the ISA memory space the register should contain a value of 0D10.

After setting the DPRAM Memory Base address, the DPRAM_EN# bit in the Board Control Register must be set to a value of 0. This enables the DPRAM for the ISA bus. The DPRAM is disabled by default on power-up or ISA reset.

Caution: Do not chose an address that conflicts with any other PC memory mapped peripheral. Disable any host PC memory managers from accessing this memory space to avoid corruption of memory.

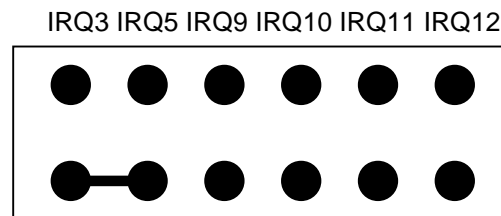
Interrupt Register

I/O base address + 4

The PC host uses the interrupt register to interrupt the DSP or clear an interrupt from the DSP to the PC. A write to this address causes control logic on the board to deliver a pulse to the DSP's /INT1 interrupt line. A read of this address clears a DSP to PC interrupt.

6.1.2. ISA Interrupt Select

The interrupt sent to the PC is determined by jumper block JP2 as one of six ISA Interrupt lines (IRQ3,5,9,10,11,12). A jumper installed interrupts the ISA bus on the associated IRQx line. No jumper is installed by default.



Default Setting Shown: No IRQ selected

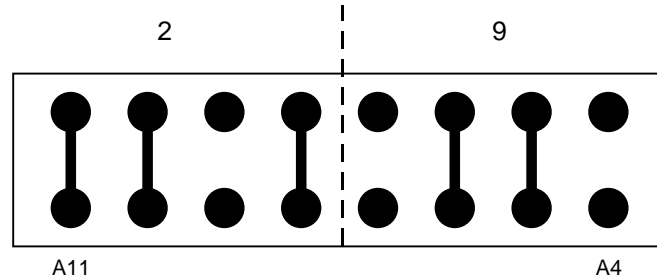
Figure 8 ISA Interrupt Select Jumper Block

6.1.3. Interrupt Handling

Interrupt Scheme	Description
To interrupt the PC from the DSP	<ol style="list-style-type: none"> 1) Set Jumper block JP2 for the desired IRQ. 2) DSP writes to the Interrupt Register at 0x700000 to cause an interrupt. 3) Host PC reads Interrupt Register at I/O base +4 to clear interrupt.
To interrupt the DSP from the PC	<ol style="list-style-type: none"> 1) The Host writes the Interrupt Register at I/O base +4 to cause the interrupt on INT1. 2) The DSP does not have to clear it as it is an edge triggered interrupt.

6.1.4. ISA Base Address Select

Jumper block JP1 selects the ISA bus base address for the board according to address lines (SA[11..4]).



Notes:

- Default Setting Shown: 0x290 (jumper in = logic 0)
- This view is different than Figure 1; it shows the jumpers upside-down.

Figure 9 ISA Base Address Jumper Block

6.2. JTAG Port

The DSP's JTAG port allows an external debugging system, such as Texas Instruments' XDS series of debug systems, to be connected to the F3 Processor Board's TMS320C32 DSP. The connector is a 2 x 6 un-shrouded header with 0.100" pin spacing as per Texas Instruments' specification.

Table 5 JTAG Connector Pinout

Pin	Signal	Pin	Signal
1	EMU1	2	GND
3	EMU0	4	GND
5	EMU2	6	GND
7	VCC	8	KEY (Absent)
9	EMU3	10	GND
11	H3 clock from C32	12	GND

6.3. Serial Port

The serial port connector consists of a 2 x 10 shrouded header with 0.100" pin spacing. It is buffered through an 8-bit 3-state noninverting buffer/line. Information about 'C32 serial port operation can be found in the *TMS320C3x User's Guide*.

Device Logic 74FCT541

Drive $V_{OH} = 3.0$ (typ) $I_{OH} = -15$ mA

Characteristics $V_{OL} = 0.3$ (typ) $I_{OH} = 64$ mA

The following figure shows the serial port interface circuit.

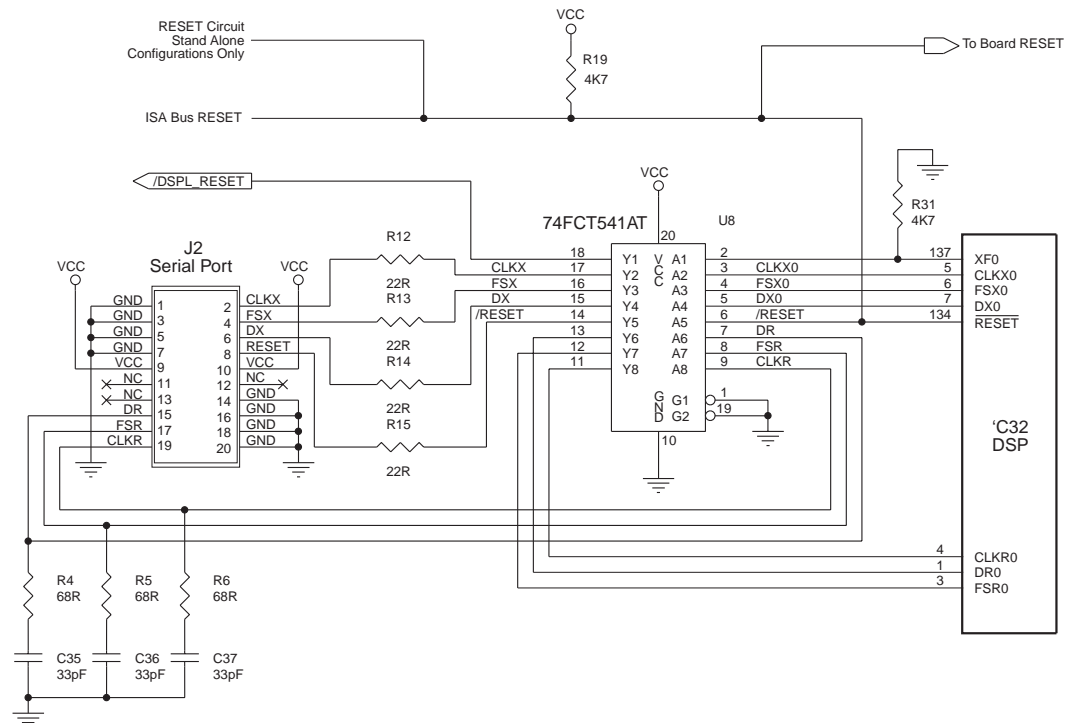


Figure 10 Serial Port Interface Circuit

Table 6 Serial Port Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	CLKX (OUT)
3	GND	4	FSX (OUT)
5	GND	6	DX (OUT)
7	GND	8	RESET# (OUT)
9	VCC (+5V)	10	VCC (+5V)
11	No Connect (NC)	12	No Connect (NC)
13	No Connect (NC)	14	GND
15	DR(IN)	16	GND
17	FSR (IN)	18	GND
19	CLKR (IN)	20	GND

6.4. Digital I/O Interface

The Digital I/O Interface supports up to 32 TTL-level digital I/O lines on a 2 x 20 shrouded header with .100" pin spacing. It can be configured as either 16 bits of latched output and 16 bits of buffered input data, or as 32 bits of buffered input data. When set for input/output mode, data on the output latch is read as part of the input data. By default, the interface is set to input mode with the output latch disabled. This interface is memory mapped in the DSP's address space and consists of a 16-bit data transceiver and a 16-bit buffer. The TCLK0, TCLK1, and /INT2 pins from the DSP are also buffered and available to the Digital I/O Interface.

The following table shows how the digital I/O interface is accessed from the 'C32 DSP.

Table 7 Digital I/O Interface accesses

Access	Address	Action
Write	0x200000	Latches D15..D0 for output.
Read	0x200000	Reads 32 bits of data: <ul style="list-style-type: none"> D15..D0 are latched output data. D31..D16 are data from digital I/O connector.
Write	0x220000	Disables the output latch.
Read	0x220000	Reads 32 bits of data from digital I/O connector.

Table 8 Digital I/O Connector Pinout

Pin	Signal	Pin	Signal
1	VCC	2	GND
3	IO1	4	I1, INT
5	IO2	6	I2
7	IO3	8	I3
9	IO4	10	I4
11	IO5	12	I5
13	TCLK0 (IN)	14	GND
15	IO6	16	I6
17	IO7	18	I7
19	IO8	20	I8
21	IO9	22	I9
23	IO10	24	I10
25	IO11	26	I11
27	TCLK1 (OUT)	28	GND
29	IO12	30	I12
31	IO13	32	I13
33	IO14	34	I14
35	IO15	36	I15
37	IO16	38	I16
39	GND	40	VCC

6.5. DSP~LINK3 Interface

The F3 Processor Board is a DSP~LINK3 master board that can support up to 4 slave DSP~LINK3 devices. Therefore, if a DSP~LINK3 module is installed on the F3 Processor Board, up to 3 additional devices can be connected to the ribbon connector J4; otherwise, up to 4 devices can be connected to J4.

The DSP~LINK3 interface consists of two 16-bit bi-directional buffers, a 16-bit address latch, and a control signal buffer. The control signals are terminated via pull down/up line resistor networks (RN1 and RN2).

6.5.1. Transfer Modes

The F3 Processor board supports the three data transfer modes and the address page turn (/ASTRB) cycle of the DSP~LINK3 interface. The timing of the DSP~LINK3 interface for the F3 Processor board is based on multiples of the DSP's H1 clock. For example, the length of a Standard Fast transfer DSP~LINK3 /DSTRB (data strobe) signal is 2 times the DSP's H1 clock signal. If a H1 cycle is about 33 ns, for the 60MHz DSP, then a Standard Fast transfer /DSTRB cycle is about 66 ns. The following table describes the different transfer modes of the interface.

Table 9 DSP~LINK3 Transfer Modes

Transfer Cycle	Description
Standard	For slave boards that are similar to DSP~LINK1 slave boards and operate with a fixed, minimum 130 ns access time. /DSTRB cycle is 5 times H1.
Standard Fast	For DSP~LINK3 slave boards that have fast, fixed access times. /DSTRB cycle is 2 times H1.
RDY Controlled	For DSP~LINK3 slave boards that require variable length access times. /DSTRB is active until the slave asserts the DSP~LINK3 ready signal (/RDY) to end the cycle.
/ASTRB Cycle	For slave boards that require more than the 16 KWords of addressing provided by the standard DSP~LINK3 address lines. The bus master uses the /ASTRB cycle to place the page address onto the DSP~LINK3 data lines. It determines which address page is accessed on the slave board. This allows access to up to 2^{14} address pages with each address page having an address depth of 2^{14} . The /ASTRB Cycle has the same timing as the Standard Fast transfer cycle.

6.5.2. Reset Operation

The DSP~LINK3 reset line (/RESET) is controlled by the DSP's XF0 line. The reset line is asserted by either a board reset condition, or by configuring the IOF register of the DSP to output a "0" on DSP's XF0 line.

A DSP~LINK3 reset should be asserted for at least 1 μ s to guarantee that it resets the DSP~LINK3 module.

6.5.3. Connector Pinouts

Connector pinouts for the DSP~LINK3 module and ribbon cable connectors are given in the following tables.

Table 10 DSP~LINK3 Ribbon Cable Connector Pinout

Pin #	Signal	Pin #	Signal
1	VCC 1	2	A15
3	A14	4	A13
5	A12	6	A11
7	A10	8	A9
9	A8	10	A7
11	A6	12	A5
13	A4	14	A3
15	A2	16	A1
17	A0	18	R/W_
19	/RESET	20	GND
21	/DSTRB	22	GND
23	/ASTRB	24	GND
25	/RDY	26	GND
27	/INT0	28	GND
29	/INT1	30	GND
31	/INT2	32	GND
33	/INT3	34	GND
35	D31	36	D30
37	D29	38	D28
39	D27	40	D26
41	D25	42	D24
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	D15	52	D14
53	D13	54	D12
55	D11	56	D10
57	D9	58	D8
59	D7	60	D6
61	D5	62	D4
63	D3	64	D2
65	D1	66	D0
67	GND	68	RSVD

Table 11 DSP~LINK3 Module Connector Pinout

Pin	Signal	Pin	Signal
1	VCC (+5 V)	35	A15
2	A14	36	A13
3	A12	37	A11
4	A10	38	A9
5	A8	39	A7
6	A6	40	A5
7	A4	41	A3
8	A2	42	A1
9	A0	43	R/W_
10	/RESET	44	GND
11	/DSTRB	45	GND
12	/ASTRB	46	GND
13	/RDY	47	GND
14	/INT0	48	/INT2
15	/INT1	49	/INT3
16	D31	50	D30
17	D29	51	D28
18	D27	52	D26
19	D25	53	D24
20	D23	54	D22
21	D21	55	D20
22	D19	56	D18
23	D17	57	D16
24	D15	58	D14
25	D13	59	D12
26	D11	60	D10
27	D9	61	D8
28	D7	62	D6
29	D5	63	D4
30	D3	64	D2
31	D1	65	D0
32	RSVD	66	RSVD
33	VCC (+5 V)	67	VCC (+5 V)
34	+12 V (unfiltered)	68	-12 V (unfiltered)

7 Specifications

Parameter	Value
Weight	136 grams (0.300 lb)
Current Consumption (Typical with no external peripherals connected)	
@5V	600 mA
@12 V	0 mA
@-12 V	0 mA
Height	11.9 cm (4.7")
Length	19.1 cm (7.5")