



***DSP-LINK3***  
**Memory Mapped Expansion Bus  
Interface Specification**

Revision 1.02

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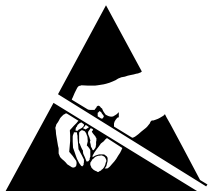
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# Preface

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# 1 Introduction

DSP~LINK3 is the generic name given to the memory mapped expansion bus that interfaces to adjacent slot I/O cards on processor boards. DSP~LINK3 is a *single master*, multiple slave bus that is typically connected using low cost high density ribbon cable. A DSP~LINK cable can have several connections or “drops” that allow a single DSP~LINK3 Master to interface to several DSP~LINK3 Slaves.

DSP~LINK3 is intended as a low latency, low interrupt latency interface for low to medium speed I/O. Since there is only a single master in any system, there is no arbitration overhead, and interrupts from DSP~LINK3 are generally directly connected to the host DSP providing low interrupt latency. With a maximum throughput of 40 MBytes/sec, and typical usable throughput of 10-20 MBytes/sec, DSP~LINK3 may not be the best choice for a high speed data pipeline.

DSP~LINK3 is NOT directly backwards compatible with DSP~LINK 1 and 2, however a DSP~LINK2 slave could be used with a DSP~LINK3 master with a paddle board to mate the connector pinouts. A DSP~LINK2 master may not work with DSP~LINK3 slaves.

## 1.1. Purpose of Document

This document provides the specification for DSP~LINK3.

## 1.2. Intended Audience

This document represents the Interface Control Drawing for the DSP~LINK3 interface. It is intended for use by Spectrum personnel, partners, and sub-contractors designing DSP~LINK3 Master or Slave interface boards.

## 1.3. Scope

This specification details mechanical specification, electrical specification, and timing **at the connector on the DSP~LINK3 Master Board**. It is the responsibility of the DSP~LINK slave board designer to ensure that the specifications defined here are met. This may involve considerations such as number of boards per system, number of capacitive loads per system, and length of cable.

## 1.4. Definition of Key Terms

DSP~LINK Master	A DSP~LINK Master drives the strobes, reset, and addresses. There must be only one DSP~LINK Master in any system.
DSP~LINK Slave	A device connected to the DSP~LINK Master through ribbon cable or backplane that provides I/O functionality to a DSP or system of DSPs. There can be multiple DSP~LINK slaves in a system.

## 2 Pin Descriptions

**Table 1 Pin Descriptions**

I/O	Pin Name	Function
O	A15..A0	Buffered DSP word address lines. Upper two address lines indicate which board is being accessed giving a maximum slave board count of 4. Byte addressing is not explicitly supported by DSP~LINK3. Each address defines a 32 bit data word, some bits of which are driven low by the slave board to allow for 16 and 8 bit data.
BIDIR	D31..D0	Buffered bi-directional DSP data lines use to read or write data to the slave card. For 16 bit DSP~LINK3 slaves, the relevant data lines should be mapped to D31..D16 for ease of handling 2's complement data. The lower DSP~LINK3 data lines should be driven low by the slave on data reads so that masking by the DSP is not required.
O	/ASTRB	Address Strobe. For DSP~LINK3 slave boards that require more than 16kwords of addressing, /ASTRB is used to latch an upper address page register. Refer to the DSP~LINK3 Timing section for operation.
O	/DSTRB	Data Strobe access. The falling edge of /DSTRB indicates that the address is valid, and that the DSP~LINK3 slave can drive the data lines for READs. The address is guaranteed to be stable while /DSTRB is low. The rising edge of /DSTRB is expected to be used to latch the data lines for WRITEs.
O	R/W_	The R/W_ line is used to indicate to the slave whether the access is a read or write cycle. A logic high indicates READ and a logic low indicates WRITE. This signal could be used to set the direction of the data buffers.
I	/INT3..0	The four interrupt lines are active low, open collector signals that are bussed to all boards in a system. The interrupts are level triggered.
I	/RDY	Tri-States Ready Signal. Used for RDY controlled cycle length accesses. The master waits for /RDY to be asserted before terminating the cycle in RDY controlled mode. /RDY is asynchronous to all master timing signals and must be re-synchronized by the master before use.
O	/RESET	Buffered active low reset signal is used to reset peripheral cards.
-	VCC	Used to provide power to small standalone test modules. 250 mA maximum current draw. DSP~LINK3 Slave boards that have their own power supply must not connect $V_{cc}$ .
-	GND	
-	RSVD	Pin(s) reserved for future use.



## 3 Operation

There are three modes of operation for DSP~LINK3 masters.

**RDY Controlled** transfers are for DSP~LINK3 slave cards that require variable length access times.

**Standard** transfers are for slave cards that are similar to DSP~LINK1 slave cards and operate with a fixed minimum 130 ns access time.

**Standard FAST** transfers are for highly specialized DSP~LINK3 slave cards that have fast, fixed access time. Only Standard Fast transfers can approach the 40 MBytes/sec data transfer capability of the DSP~LINK3 bus.

### 3.1. RDY Controlled Transfers

DSP~LINK3 slave cards like the IndustryPack® Module Carrier Boards are expected to require RDY controlled transfers between the DSP~LINK3 Master processor card and the IP Carrier DSP~LINK3 slave card.

The sequence of events for a RDY Controlled transfer is as follows:

**Table 2 RDY Controlled Transfer**

Master	Slave
Drives Address and R/W_ lines	
	Decodes upper two address bits. If address = own, then output enable /RDY
Assert /DSTRB to indicate type of transfer	
	Slave uses /DSTRB low and address to turn on data bus transceivers. Direction is set by R/W_. Slave re-synchronizes the strobe signals for use in state machine.
	State machine performs required access.
	Slave drives /RDY low when finished access.
Master re-synchronizes the ready signal, latches data on a read, releases strobe signal, and terminates the host processor cycle.	
	Slave determines that the /DSTRB has been released and returns to idle state.

1. The Slave must tri-state /RDY until the A15 and A14 address lines are valid.
2. The Slave cannot drive the data bus until /DSTRB has been asserted.

3. The Slave must not assert /RDY until /DSTRB is asserted.
4. The Slave must drive the data bus until /DSTRB has been negated by the Master.
5. The Master cannot negate /DSTRB until the Slave asserts /RDY.
6. The Slave must use the logic high condition of /DSTRB to negate /RDY.
7. The Slave must negate /RDY (drive it to a logic high) before tri-stating /RDY.

### 3.2. Standard Transfers

Simpler DSP~LINK3 slave cards such as a dedicated SRAM interface, or a register interface have no requirement for variable cycle length, so Standard transfers will be used.

**Table 3 Standard Transfer**

Master	Slave
Drives Address and R/W_ lines	
	Decodes upper two address bits. If address = own, then enable RAMs.
Assert /DSTRB	Asynchronous decode of Address, /DSTRB and R/W_ are used to drive the /WE and /OE signals
/DSTRB is asserted for a defined length of time	
Strobe signal returns high and returns to idle state.	
	For READs, /DSTRB negated turns off data bus drivers - for writes, the rising edge of /DSTRB latches data into SRAM.

### 3.3. /ASTRB Cycle

The /ASTRB Cycle is a special type of transfer that is only required for Slave Boards that require more than the 16 kWords of addressing provided by the standard A0..A13 signal lines (Note that A14, A15 are used to select the DSP~LINK3 slave board being addressed).

The timing for an /ASTRB Cycle looks the same as a Standard FAST transfer, with the following exceptions:

1. /DSTRB does not pulse low at the same time as /ASTRB. The two signals are mutually exclusive.
2. /ASTRB pulses low with timing similar to Standard FAST transfers. Refer to the DSP~LINK3 timing section for specific details. The rising edge of /ASTRB is used to latch the lower address lines into the address paging register.

3. The Slave must ignore the R/W\_ line during an /ASTRB cycle.
4. The Slave must not drive the data bus on /ASTRB cycles.
5. Data lines are “Don’t Care”.

A separate paging register should be used for each target (i.e. IndustryPack® Module site) on the slave board.

**NOTE:** A15 and A14 still must be used to select which board is being accessed during /ASTRB cycles.

### 3.4. Setup and Hold Times

For RDY controlled, Standard, and Standard Fast transfers, DSP~LINK3 will provide address setup time and address hold time for all accesses, and data hold time for writes. /DSTRB will return high on back to back read or write transfers for direct interface to FIFOs. This is significant because the TMS320C4x and TMS320C3x /STRBx signal does not return high on back to back reads. This functionality may have to be specifically designed in for DSP~LINK3 Masters. Refer to the DSP~LINK3 Timing section for details.



## 4 DSP~LINK3 Timing

### 4.1. Timing Parameters For All Cycles

Table 4 Timing Parameters For All Cycles

Parameter	Description	Standard	Standard FAST	RDY Controlled
t asu	Address Setup Time before /DSTRB asserted	15 ns min.	15 ns min.	15 ns min.
t ah	Address Hold Time after /DSTRB negated	10 ns min.	10 ns min.	10 ns min.
t r/wsu	R/W# Setup Time before /DSTRB asserted	15 ns min.	15 ns min.	15 ns min.
t r/wh	R/W# Hold Time after /DSTRB negated	10 ns min.	10 ns min.	10 ns min.
t dv	Data Valid after /DSTRB asserted on write	10 ns max.	10 ns max.	10 ns max.
t dhw	Data Hold Time after /DSTRB negated on write	10 ns min.	10 ns min.	10 ns min.
t acc	Data Access Time after /DSTRB asserted on read	100 ns max.	35 ns max.	N/A
t dsu	Data setup time before /RDY low	N/A	N/A	0 ns min.
t dhr	Data Hold Time after /DSTRB negated on read	0 ns min.	0 ns min.	0 ns min.
t dhiz	Data High-Z after /DSTRB negated on read	15 ns max.	15 ns max.	15 ns max.
t pw	/DSTRB asserted pulse width <sup>Note 1</sup>	130 ns min.	45 ns min.	N/A <sup>Note 3</sup>
t rec	/D(A)STRB negated between back to back accesses	45 ns min.	45 ns min.	45 ns min.
t ddis	Data High-Z by Master before /DSTRB asserted on read	0 ns min.	0 ns min.	0 ns min.
t rdyh	Delay, /DSTRB High to /RDY high <sup>Note 2</sup>	N/A	N/A	0 ns min. 15 ns max.
t rdyhiz	/RDY tri-state after address change	N/A	N/A	15 ns max.
t asuA	Address Setup Time before /ASTRB <b>rising edge</b>	N/A	15 ns min.	N/A
t ahA	Address Hold Time after /ASTRB <b>rising edge</b>	N/A	10 ns min.	N/A
t pwA	/ASTRB asserted pulse width	N/A	45 ns min.	N/A
t rst	/Reset Pulse Width	1 $\mu$ s min.	1 $\mu$ s min.	1 $\mu$ s min.

DSP~LINK3 slaves that support Standard FAST transfers must meet the timing requirements in this table with considerations for ribbon cable length and number of loads.

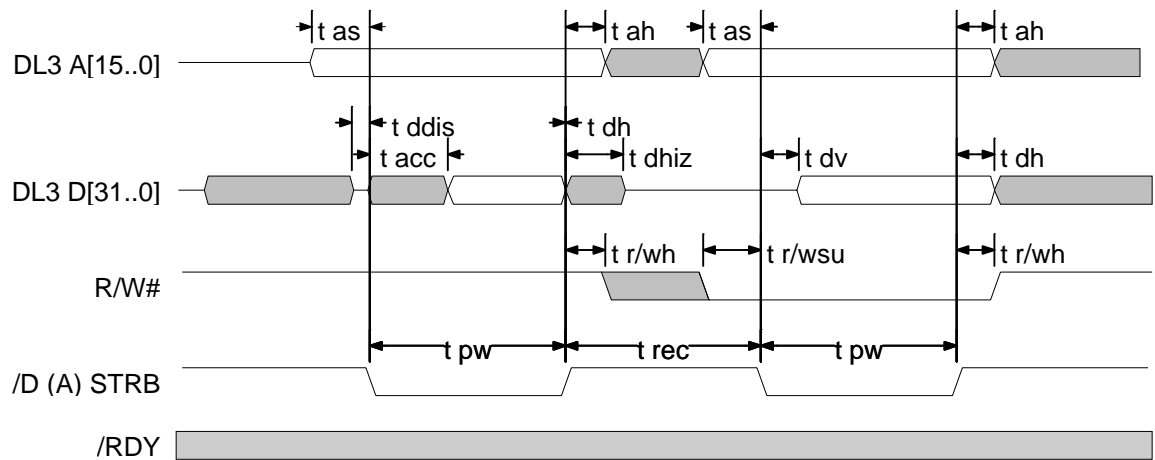
Notes:

1. It is expected that some DSP~LINK3 Masters will be unable to transfer data at the Standard FAST 40 MBytes/sec transfer rate. DSP~LINK3 Masters that cannot

provide 10 MHz (32 bit) transfers to Standard FAST Slaves must still meet all of these timing parameters.

2. /RDY must be DRIVEN high before tri-stated. The intention is for /RDY to be driven high by the slave board with combinatorial logic when /DSTRB negated, and /RDY to be tri-stated when the board address bits change. While the address bits are changing, there will be a period of time when two boards will be driving /RDY, however the timing guarantees that neither will drive /RDY low, so contention is avoided.
3. There is no minimum or maximum pulse length for /DSTRB during a /RDY Controlled Cycle. The constraints on /DSTRB are such that it cannot return high until /RDY has been asserted, so the pulse length is dictated by the DSP~LINK3 Slave. DSP~LINK3 Masters have no requirement to implement a timeout for /RDY Controlled accesses that do not complete.

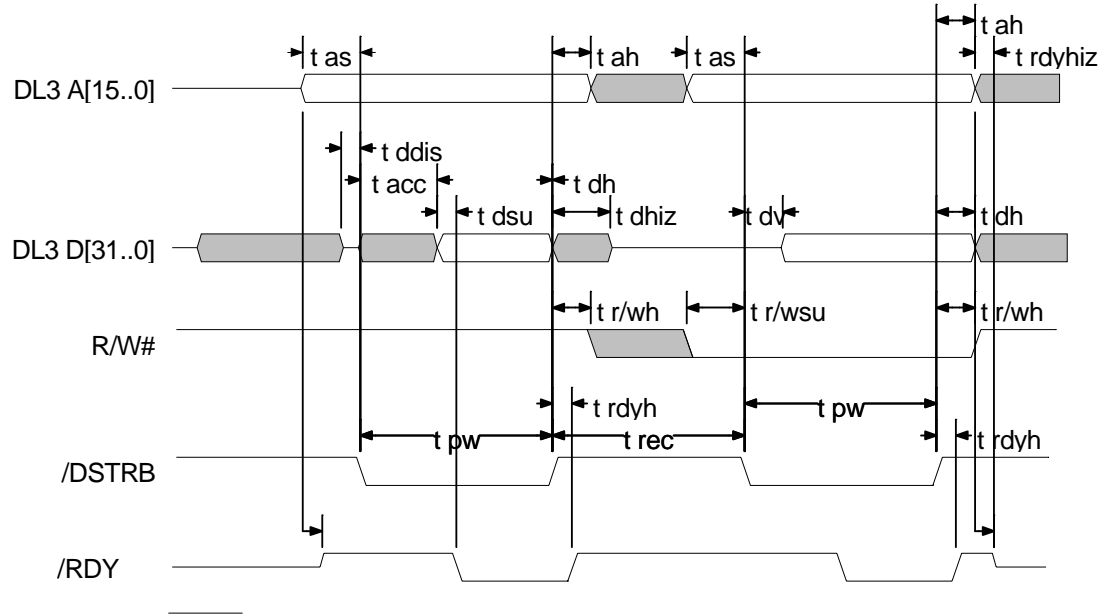
## 4.2. Standard and Standard FAST Access



**Figure 1 Standard and Standard FAST Access Timing**

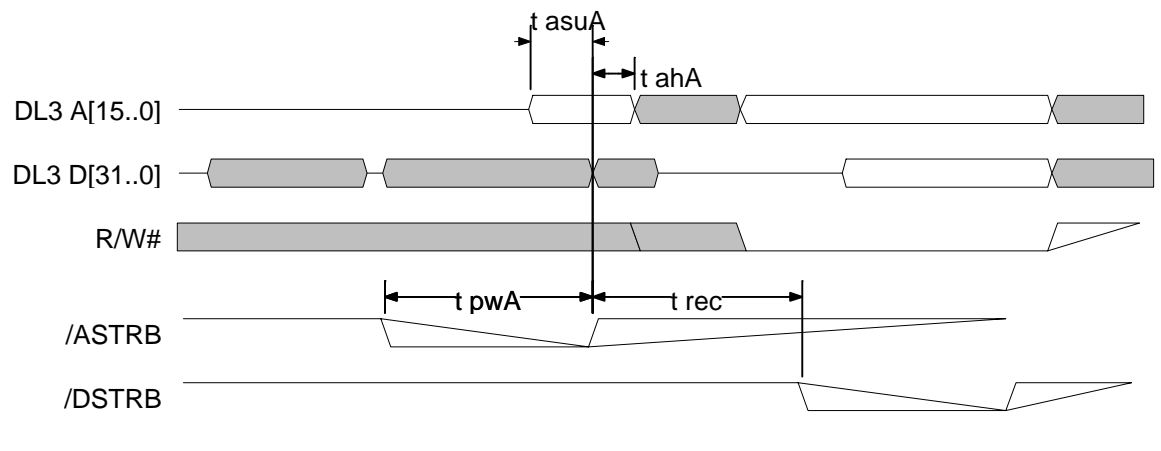
### 4.3. RDY Controlled Cycles

This diagram shows /RDY tri-stated when the address does not match any slave board, however the SCSI-2 style terminators will keep the voltage at ~3V.



**Figure 2 RDY Controlled Cycle Timing**

### 4.4. /ASTRB Cycle



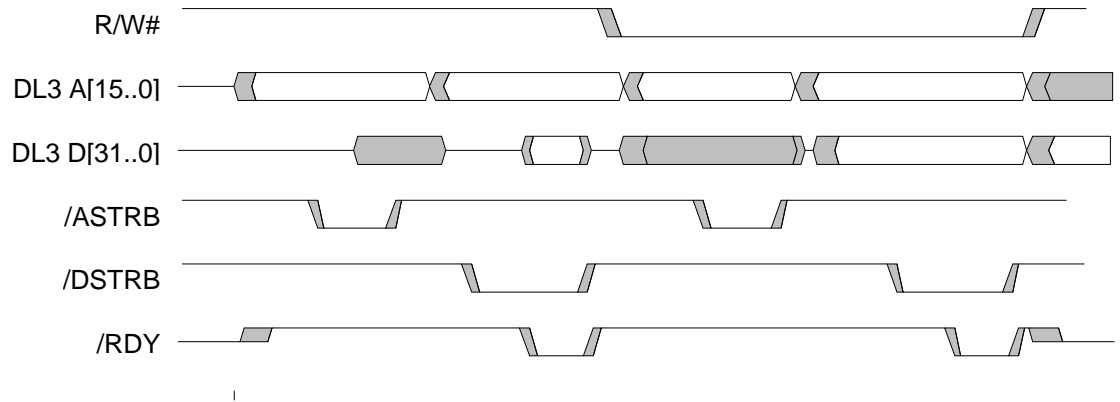
**Figure 3 /ASTRB Cycle Timing**

The /ASTRB timing varies from the /DSTRB timing in address setup time. Since the rising edge of /ASTRB is used to latch the lower address lines, address setup time is only defined for the rising edge. This will allow Master boards to be designed with fewer cycles (less overhead) required for /ASTRB cycles. This constraint should not affect the design of Slave boards. The

/DSTRB cycle following an /ASTRB cycle can be Standard, Standard FAST, or /RDY Controlled.

#### 4.5. Example of /ASTRB Use for Extended Addressing

The following diagram shows operation of sequential /ASTRB and /DSTRB accesses from a 60 MHz TMS320C40 Master to a /RDY controlled slave. A system that would require accesses of this type would be a FLASH memory DSP~LINK3 Slave board with more than 16Kwords of memory.



**Figure 4 /ASTRB Operation Timing**

**NOTE:** This diagram is a sample implementation for demonstration purposes only. No specific timing information should be implied.

---

# 5 Electrical and Mechanical Specifications

## 5.1. Primary Interface (Ribbon Cable)

### 5.1.1. Board Connector:

**AMP 1-104068-8** Shrouded vertical through-hole plug. 2x34 positions with 0.1"x0.050" pin spacing.

### 5.1.2. Cable Connector:

**AMP 1-111196-7** 0.025" ribbon cable mount receptacle. 2x34 positions with 0.1"x0.050" socket spacing

### 5.1.3. Ribbon Cable Length

The ribbon cable length must be kept to less than or equal to twelve inches (30 centimetres).

## 5.1.4. Connector Pinout

**Table 5 Connector Pinout**

Pin #	Signal	Pin #	Signal
1	V <sub>cc</sub> <sup>1</sup>	2	A15
3	A14	4	A13
5	A12	6	A11
7	A10	8	A9
9	A8	10	A7
11	A6	12	A5
13	A4	14	A3
15	A2	16	A1
17	A0	18	R/W_
19	/RESET	20	GND
21	/DSTRB	22	GND
23	/ASTRB	24	GND
25	/RDY	26	GND
27	/INT0	28	GND
29	/INT1	30	GND
31	/INT2	32	GND
33	/INT3	34	GND
35	D31	36	D30
37	D29	38	D28
39	D27	40	D26
41	D25	42	D24
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	D15	52	D14
53	D13	54	D12
55	D11	56	D10
57	D9	58	D8
59	D7	60	D6
61	D5	62	D4
63	D3	64	D2
65	D1	66	D0
67	GND	68	RSVD

1) V<sub>cc</sub> is intended to be used as a presence detect or for powering very small test modules. Current drive capability is limited to 250 mA. DSP~LINK3 Slave boards that have their own power supply **MUST NOT** connect Pin 1: V<sub>cc</sub>.

## 5.2. Secondary Interface (P2 on VME Boards)

On VME processor boards, DSP~LINK3 will optionally be routed to the P2 connector using rows A&C. The P2 interface would be a secondary connection - Master and slave boards must support the ribbon cable interface as the primary connection, however there is no requirement for *simultaneous* ribbon cable and P2 interface on any single DSP~LINK Master or Slave. If the P2 interface is used, then the ribbon cable interface will not be used. Potentially, both interfaces could use the same physical transceivers.

### 5.2.1. P2 Connector Pinout

Table 6 P2 Connector Pinout

Row A	Signal	Row C	Signal
1	Reserved	1	A15
2	A14	2	A13
3	A12	3	A11
4	A10	4	A9
5	A8	5	A7
6	A6	6	A5
7	A4	7	A3
8	A2	8	A1
9	A0	9	R/W_
10	/RESET	10	GND
11	/DSTRB	11	GND
12	/ASTRB	12	GND
13	/RDY	13	GND
14	/INT0	14	/INT2
15	/INT1	15	/INT3
16	Reserved	16	Reserved
17	D31	17	D30
18	D29	18	D28
19	D27	19	D26
20	D25	20	D24
21	D23	21	D22
22	D21	22	D20
23	D19	23	D18
24	D17	24	D16
25	D15	25	D14
26	D13	26	D12
27	D11	27	D10
28	D9	28	D8
29	D7	29	D6
30	D5	30	D4
31	D3	31	D2
32	D1	32	D0

### 5.3. Electrical Characteristics

**Table 7 Electrical Characteristics**

Parameter	Min.	Max.
<b>Output High Voltage (<math>V_{OH}</math>)</b>	2.4 V	
<b>Output Low Voltage (<math>V_{OL}</math>)</b>		0.55 V
<b>Input High Voltage (<math>V_{IH}</math>)</b>	2.0 V	
<b>Input Low Voltage (<math>V_{IL}</math>)</b>		0.8 V
<b>Output Low Current (<math>I_{OL}</math>)</b> Control Signals (DSTRB, ASTRB, RDY, /INTx) Address and data signals	48 mA 24 mA	
<b>Output High Current (<math>I_{OH}</math>)</b> Control Signals (DSTRB, ASTRB, RDY, /INTx) Address and data signals		-12 mA -24 mA
<b>Input Low Current (<math>I_{IL}</math>)</b>		-1 mA
<b>Input High Current (<math>I_{IH}</math>)</b>		0.5 mA
<b>Capacitive Loading per Signal</b>		50 pF

The capacitive loading per signal allows each slave to have only one load per data, address, and control line. 10 pF is the suggested maximum capacitance per DSP~LINK3 slave card, although custom implementations are limited to 50 pF for the entire bus.

### 5.4. Signal Conditioning and Termination

**Data Lines D31..D0:** 74FCT162245 type bus transceivers (or equivalent) must be used. These components provide 25Ω series resistors inline with the drivers. The inline resistors are bypassed for the receivers.

**Address Lines A15..A0:** 74FCT162245 type bus transceivers (or equivalent) must be used for DSP~LINK3 masters. These components provide 25Ω series resistors inline with the drivers. The inline resistors are bypassed for the receivers. Some DSP~LINK3 Master boards must latch the address to provide adequate timing. In this event, 74FCT162373 type transparent latches should be used.

**TTL Level Outputs (from Master), TTL Level Tri-State Inputs (to Master), and Open Collector Inputs (to Master):** The source for the control signals must use 74FCT16245 type bus transceivers (or equivalent). /RESET, /DSTRB, /ASTRB, R/W\_, /RDY, /INT0, /INT1, /INT2, and /INT3 shall have parallel termination that consists of the following:

1. SCSI-2 style 220 $\Omega$  pull-up / 330 $\Omega$  pull-down passive termination
2. or dedicated active SCSI-2 style termination. An example of an active SCSI-2 terminator is the Texas Instruments TL2218-285PWLE.

The termination must be installed at the source (Master) and at the last target (Slave) on the DSP~LINK3 cable. All slave boards must have the capability to disable the SCSI-2 style termination by removing resistor packs for passive termination or jumper disabling for active termination.



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## 6 Appendix A: DSP~LINK3 Module Definition

This appendix provides additional definition for DSP~LINK3 Modules. The intention is to provide a module specification that allows a single slot processor board with I/O solution for PCI, ISA and VME buses. The applications for DSP~LINK3 modules are not limited to these buses, however single slot solutions are achievable.

### 6.1. J1 DSP~LINK3 Module Connector & Pinout

The stacked height (PWB to PWB) can be found by adding the Module connector and Carrier Board connector height to standoff value.

**Module Connector:**

Hirose FX4C3-68S-1.27DSA (5.5 mm to standoff)

Alternate Module Connectors:

Hirose FX4C2-68S-1.27DSA (4.5 mm to standoff)

Hirose FX4C-68S-1.27DSA (2.5 mm to standoff)

**Carrier Board Connectors:**

Hirose FX4C-68P-1.27DSA (2.5 mm to standoff) (CV5)

Alternate Module Connectors:

Hirose FX4C1-68P-1.27DSA (3.5 mm to standoff) (F5)

Hirose FX4C3-68P-1.27DSA (5.5 mm to standoff)

## 6.1.1. J1 Pinout

**Table 8 J1 Pinout**

Pin	Signal	Pin	Signal
1	VCC (+5 V)	35	A15
2	A14	36	A13
3	A12	37	A11
4	A10	38	A9
5	A8	39	A7
6	A6	40	A5
7	A4	41	A3
8	A2	42	A1
9	A0	43	R/W_
10	/RESET	44	GND
11	/DSTRB	45	GND
12	/ASTRB	46	GND
13	/RDY	47	GND
14	/INT0	48	/INT2
15	/INT1	49	/INT3
16	D31	50	D30
17	D29	51	D28
18	D27	52	D26
19	D25	53	D24
20	D23	54	D22
21	D21	55	D20
22	D19	56	D18
23	D17	57	D16
24	D15	58	D14
25	D13	59	D12
26	D11	60	D10
27	D9	61	D8
28	D7	62	D6
29	D5	63	D4
30	D3	64	D2
31	D1	65	D0
32	RSVD	66	RSVD
33	VCC (+5 V)	67	VCC (+5 V)
34	+12 V (unfiltered)	68	-12 V (unfiltered)

## 6.2. I/O Connector

The I/O connector used for a DSP~LINK3 module is entirely user defined, however recommended connectors have been defined. The figures shown in the Mechanical Specifications section show the required placement of the recommended connectors for PCI, VME, and ISA cards.

### 6.2.1. PCI and ISA Cards

For PCI and ISA cards, the a right angle high density 26 pin DSUB is the recommended I/O solution that allows I/O through the PC card endplate. When the module is installed, the PC card endplate will bolt directly to the DSUB connector.

**PCI / ISA I/O Connector:** AMP 748481-6 26 pin high density (3 row) R/A D-Subminiature

### 6.2.2. VME Cards

For VME cards, a second Hirose 68 pin through-hole board to board connector is used to interface to the user defined pins on the P2 interface.

**VME I/O Connector:** Hirose FX4C3-68S-1.27DSA (5.5 mm to standoff)

Note: the required height of the I/O connector is dependent on the height of the J1 connector chosen.

## 6.3. Mechanical Specifications

DSP~LINK3 modules use a custom form factor that is optimal for PCI, ISA and VME bus module carrier boards. There are two sizes of DSP~LINK3 modules, and they are designated Type 1 and Type 2 modules.

**Note:** the Type 0 module defined in previous Revisions of this specification has been discontinued due to its small available board area.

### 6.3.1. Type 1 Module

The Type 1 Module defines the standard size, and it is expected to be used for most I/O solutions. The following figure shows the Type 1 DSP~LINK3 Module mechanical dimensions.

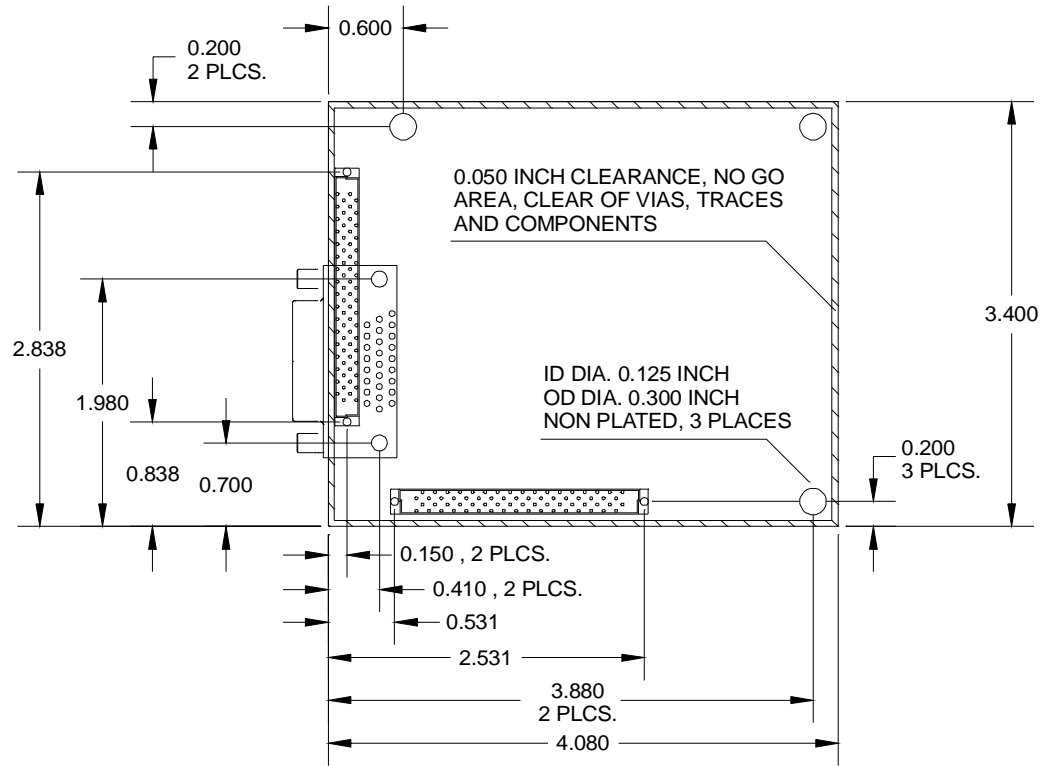


Figure 5 Type 1 DSP~LINK3 Module

## 6.4. Buffering and Termination

DSP~LINK3 Modules are not required to provide the SCSI-2 style termination for DSP~LINK3 interface control and interrupt signals. 74FCT2xxx transceivers must be used for data lines as defined in the Signal Conditioning and Termination section of this document. DSP~LINK3 modules must limit loading on the data, address, and control lines to a load of no more than 10 pF per signal. DSP~LINK3 Modules are required to provide 48 mA drive for the interrupt lines.